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EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Test and measurement special issue

In-circuit emulation

Troubleshooting analog circuits—the final chapter

US engineers in Japan

Wescon/89 preview

Standard graphics environments make application software portable

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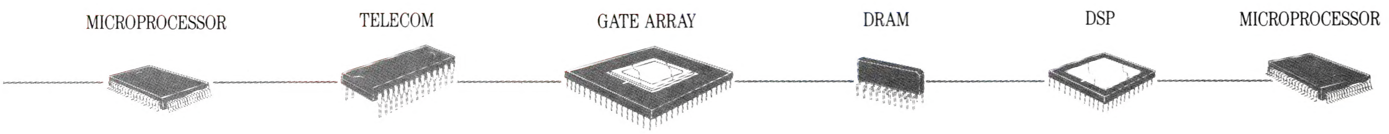

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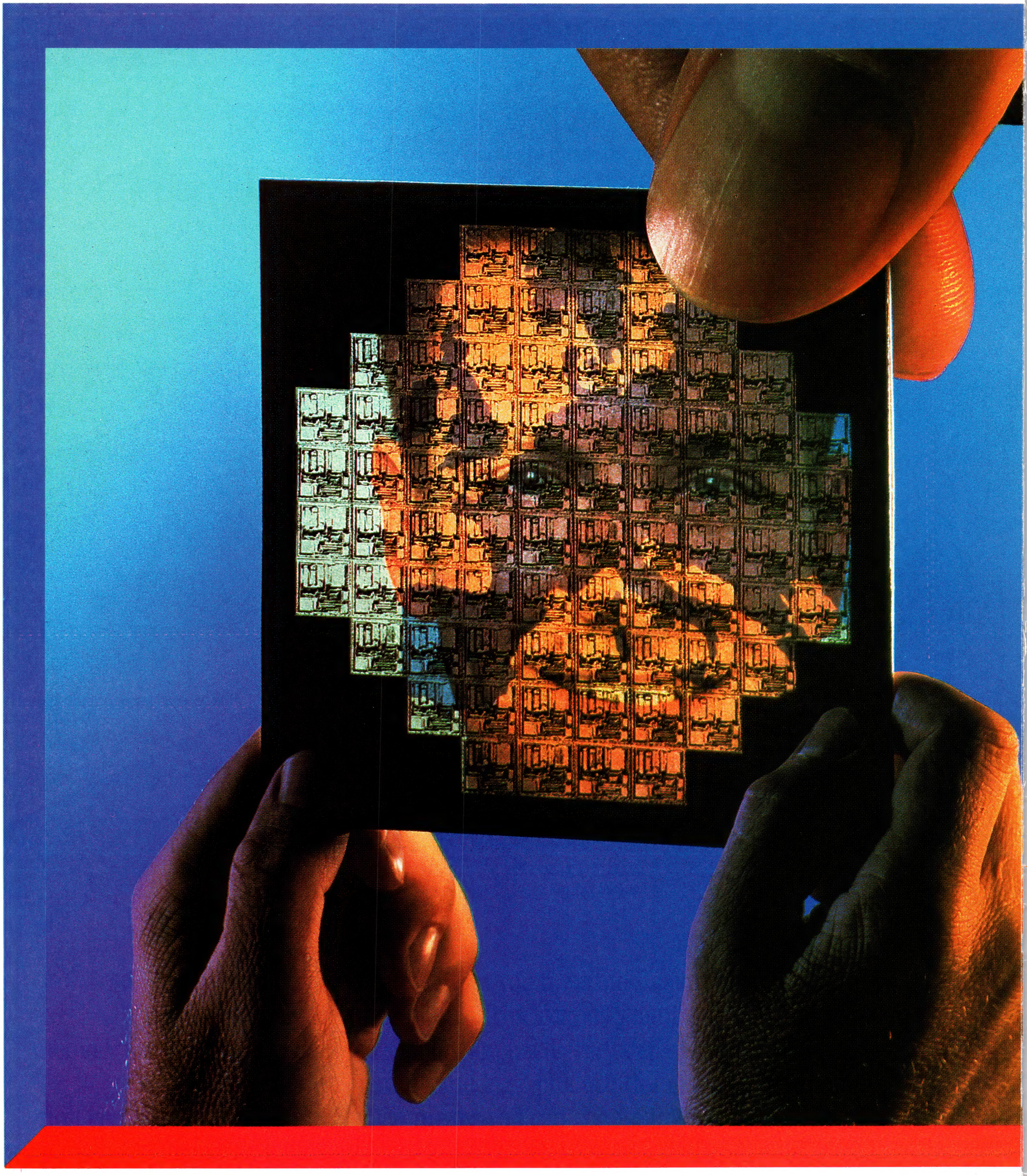

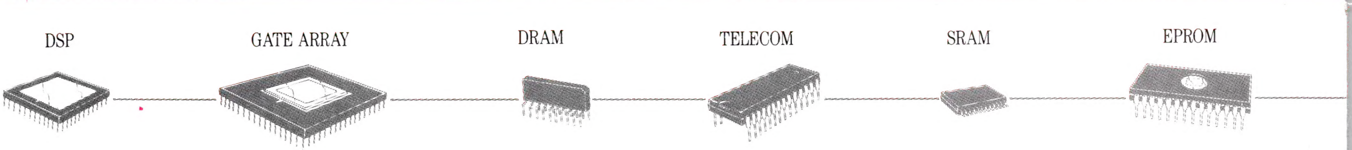
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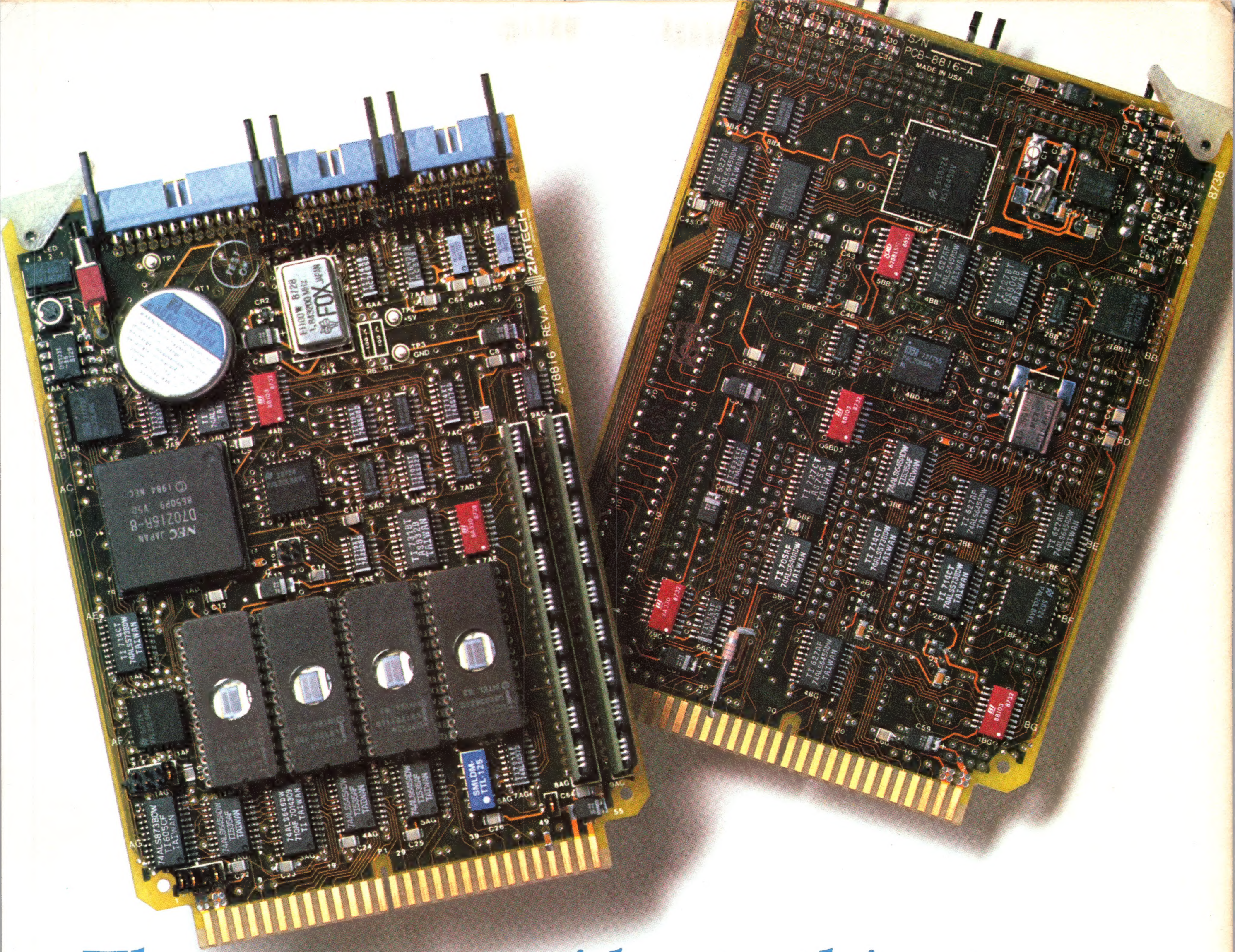

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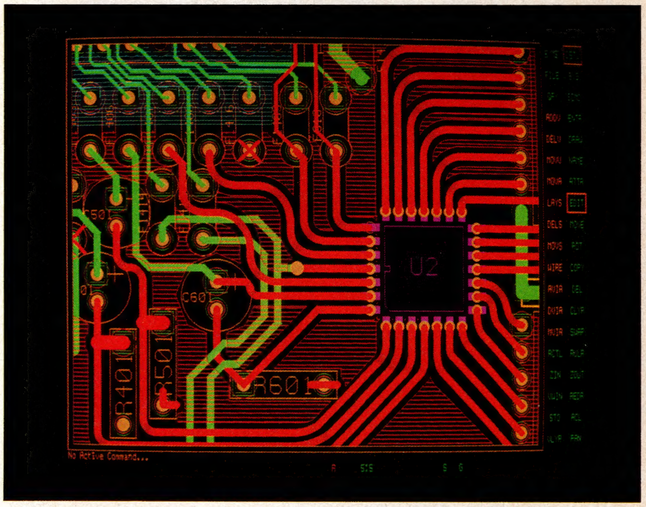

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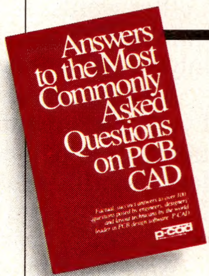

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EDN Magazine Edition

Volume 34, Number 22

October 26, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

***On the cover:** Graphics-environment standards are the key to any hope of application software portability among different systems. No single standard yet exists, and you must choose a graphics environment with care. See the Special Report, which begins on pg 152. (Photo courtesy Open Software Foundation Inc)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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BPA ABP

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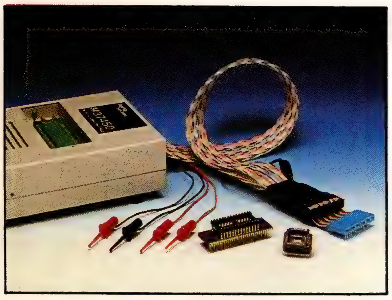

***The reports of in-circuit emulation** are greatly exaggerated. In fact, emulator manufacturers are confident that they can handle anything chip designers generate (pg 73).*

TECHNOLOGY UPDATES

Continued on page 9

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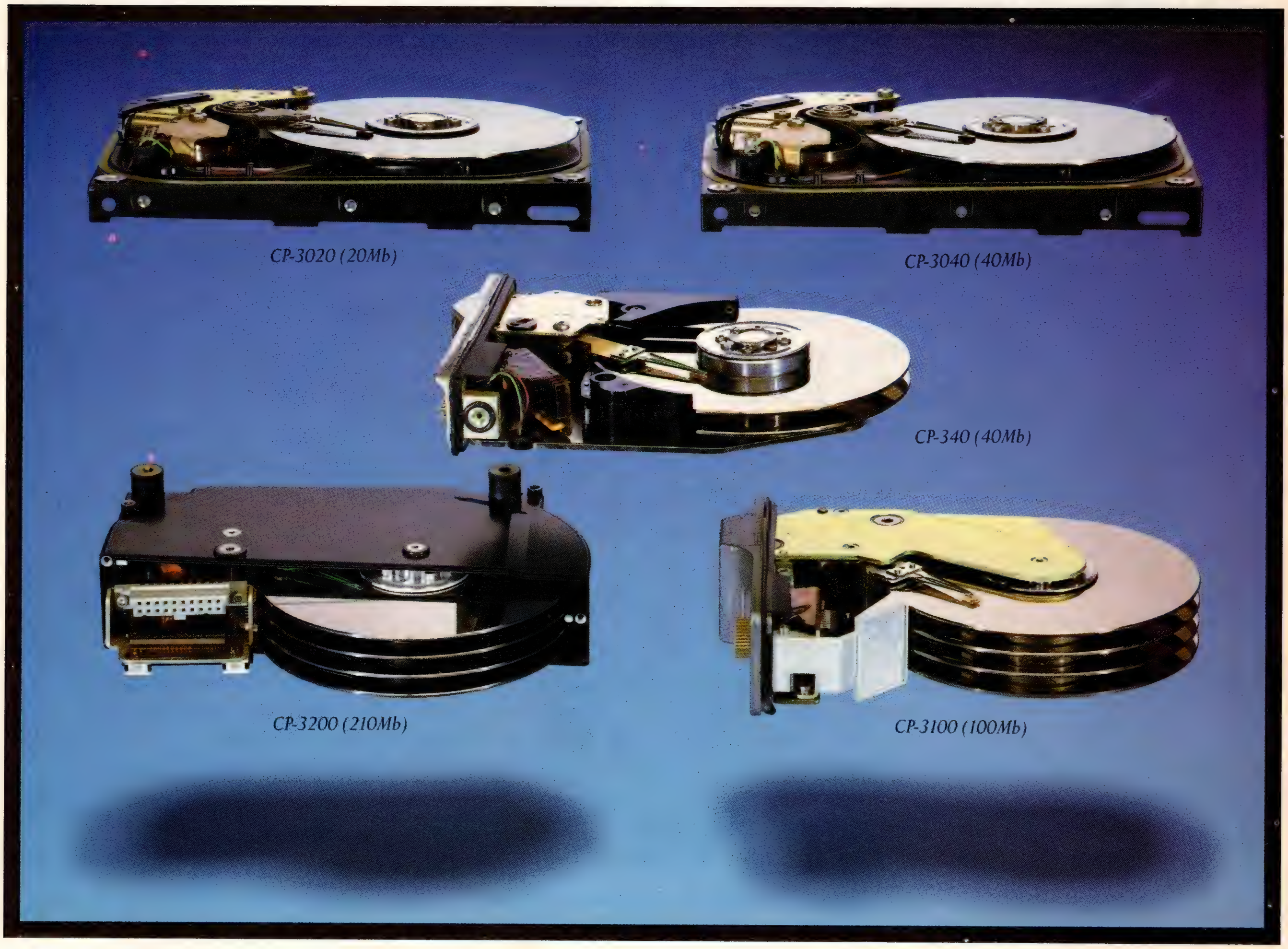
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Continued from page 7

EDN Magazine Edition®

October 26, 1989

PRODUCT UPDATES

DESIGN IDEAS

EDITORIAL 51

Gary Legg, author of EDN's series on engineers in Asia, offers some observations about playing by the rules in Japan.

NEW PRODUCTS

PROFESSIONAL ISSUES 307

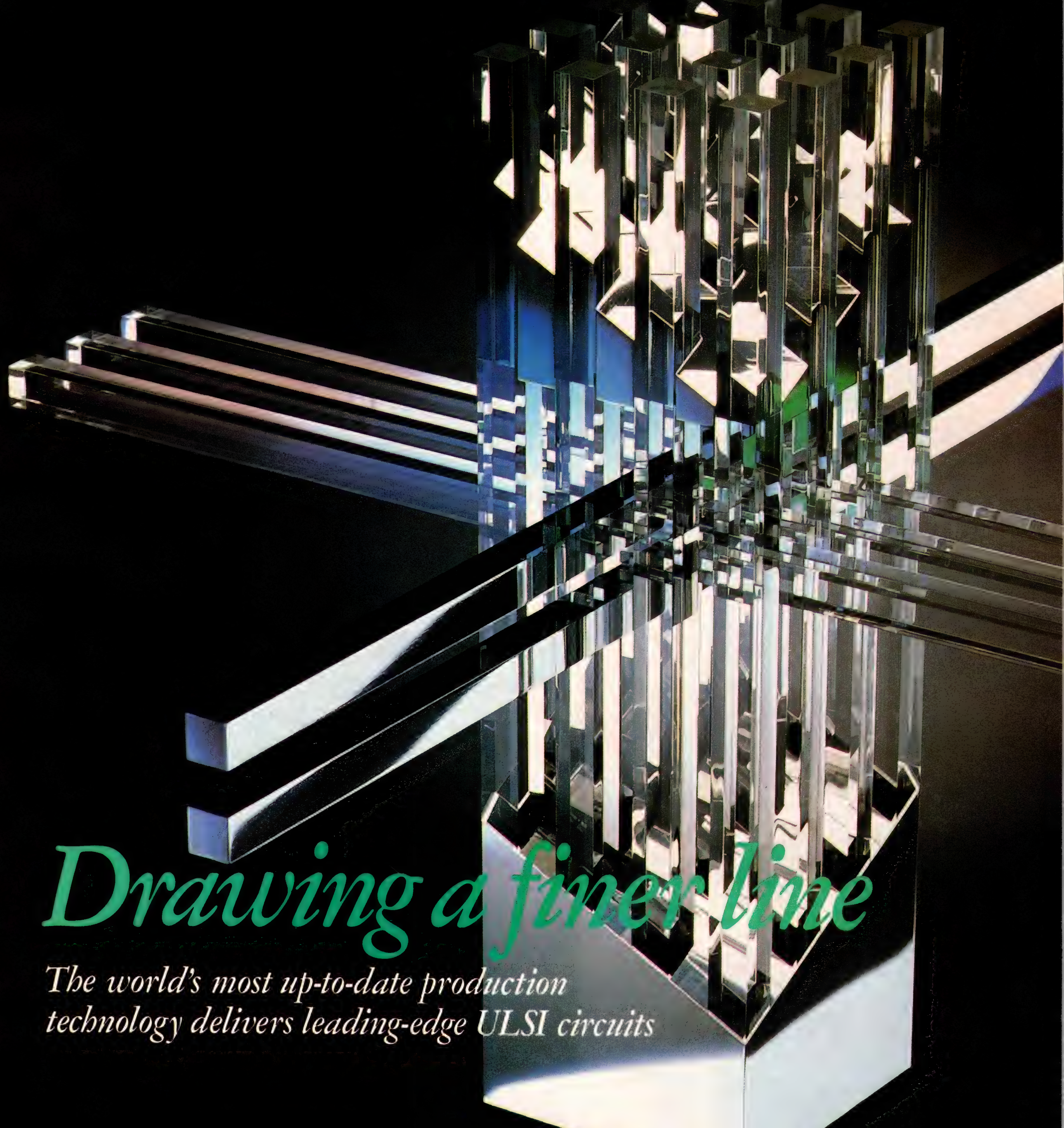
Starting over: What do you do when the company you founded goes bust? You try again.—*Jay Fraser, Associate Editor*

LOOKING AHEAD 313

Automotive market grows for discrete semiconductors . . . Software market will grow to $36 billion by 1993.

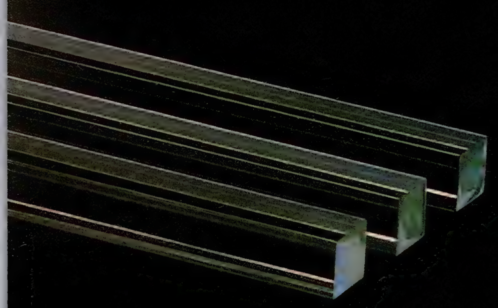
DEPARTMENTS

Finishing first has a lot to



Drawing a finer line

The world's most up-to-date production technology delivers leading-edge ULSI circuits



OKI
ELECTRONIC DEVICES

OKI SYSTEM TECHNOLOGIES.

Sub-micron production in full swing, bringing the new age of 4M DRAMs

Oki's Miyagi Plant, benefitting from the latest advances in the company's system technology, has already reached mass production and shipment of 1M-bit memories and has recently begun quantity production of 4M DRAMs. At the Miyagi Plant, broad utilization of ultra-fine process technology and state-of-the-art automation combine to assure the high quality of these products. Oki is already well underway with technological innovation enabling production of 16M-bit memories.

High-level automation with ultra-fine process production

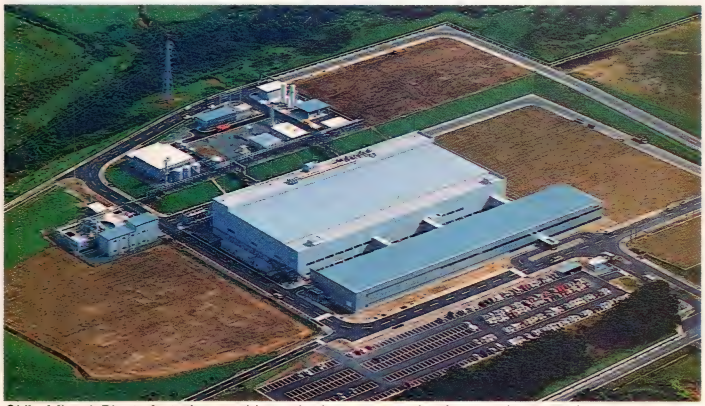
Oki's 0.8μ process technology used in its second-generation 1M- and 4M-bit memories has been integrated into one of the world's most advanced production lines for reliable mass production of over 20,000 6-inch wafers per month.

In 1988 Oki led the world with the first facility dedicated for production of sub-micron devices. Today that lead is being extended with the latest advances in automated manufacturing, such as sophisticated wafer tracking systems for improved quality and production control monitoring.

From the transportation system, driven by linear motors, to individual production equipment in each process machine group, all are computer controlled. To assure products of extremely stable quality, automation and every detail of the production environment are maintained at the world's highest levels.

High performance and packaging flexibility support customers in a wide range of applications

Oki's Advanced System Technologies are dedicated to total customer satisfaction. A comprehensive service system provides flexibility, quality, cost savings and quick turn-around times.



Oki's Miyagi Plant, featuring world-standard process technology and automation.

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So if you're thinking about a new combinational tester, make a smart call. Contact Daryl Layzer at 617-482-2706, Ext. 2808 for more information about the new L350 VLSI Board Test System.

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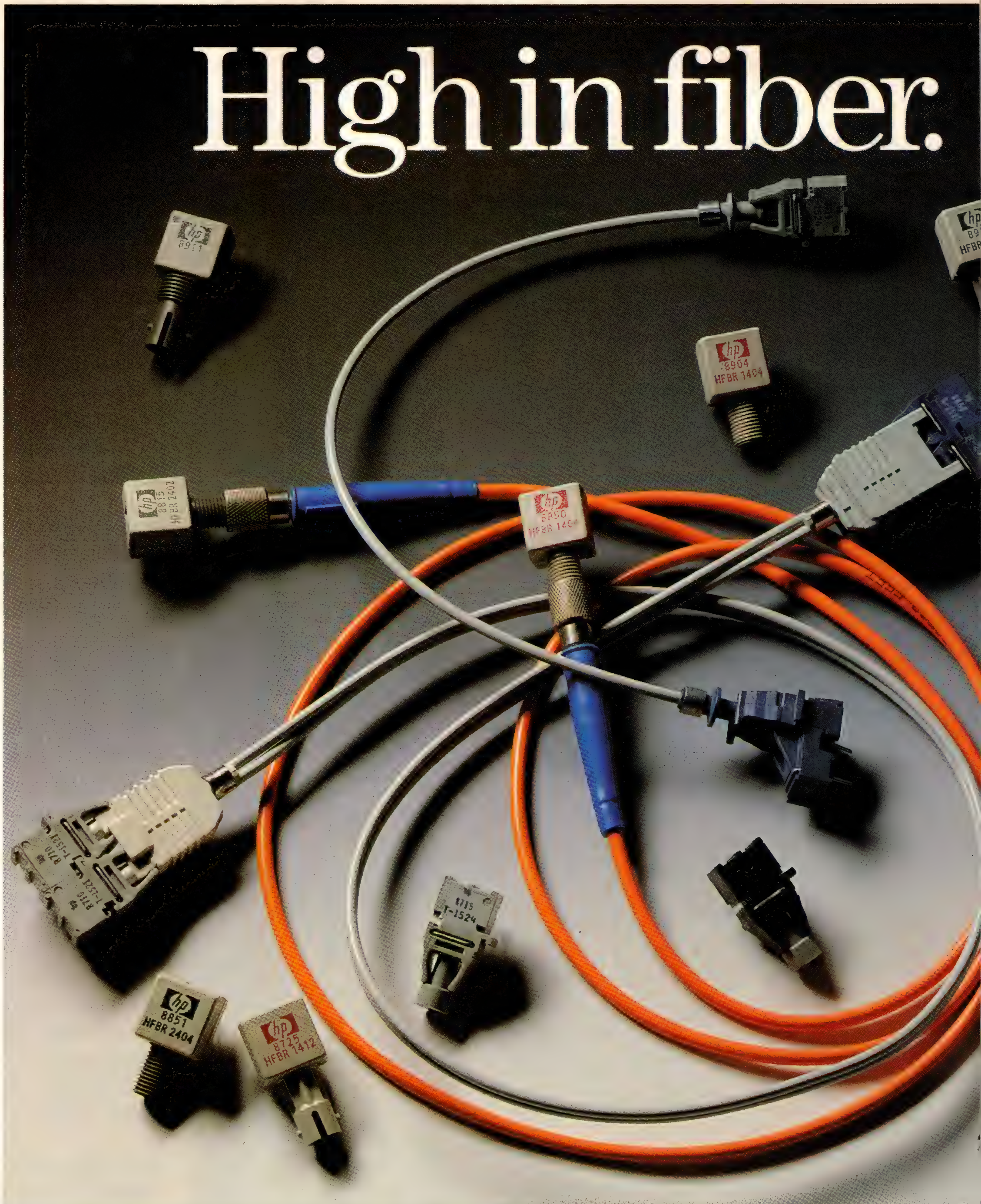
Test development today:



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NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

GRAPHICS IC INTEGRATES 8514/A AND VGA COMPATIBILITY

Early in 1990, Trident Microsystems (Sunnyvale, CA, (408) 738-3194) will ship the TAVA 9000, a single chip for IBM PC, PC/XT, PC/AT, and PS/2 systems that complies with both IBM's 8514/A and VGA graphics standards. The TAVA 9000 is register-level and applications-interface compatible with the 8514/A graphics specification and with all previous graphics standards, including VGA, EGA, CGA, MDA, and Hercules. Trident's 8514/A design integrates all the features of both the 8514/A and the company's own TVGA 8800 VGA chip, thus you can use existing graphics software without the risk of hardware conflicts. The device supports displays with resolutions of 640×480, 800×600, and 1024×768 pixels in 256 colors out of a 256,000-color palette. The TAVA 9000 will be available both as a single chip and in a board-level configuration. Prices for the 144-pin quad flatpack will range from $150 to $175. —Anne Watson Swager

CONTROLLER BOARD RUNS HIGH-LEVEL FORTH SOFTWARE

The TDS9090 4×3-in. Forth-based controller board made in England is now available in the US from the Saelig Co (Victor, NY, (716) 425-4367) for $399. The controller draws 3 mA from a 6V supply during operation, and it can run on a 9V supply for one year in standby mode. It uses a Hitachi HD63A03Y µP, 30k bytes of data RAM, and 16k bytes of program RAM for high-level Forth code. The controller also features 256k bytes of EEPROM, a watchdog timer, and a time-of-day clock. It has 35 parallel I/O ports and two RS-232C ports. A data-logging daughter card plugs into the board to provide 10 channels of A/D conversion and six channels of D/A conversion.—John Gallant

VMEBUS BOARDS OPERATE UNDER SEVERE CONDITIONS

Designers and system integrators who require computer boards that operate under severe conditions soon will be able to take advantage of the VMEbus architecture. Motorola's Microcomputer Division (Tempe, AZ, (800) 556-1234, ext 230, or (602) 438-3522) expects to offer two grades of computer boards that operate in either a severe industrial or a severe military environment. The severe industrial-grade boards will withstand temperatures within the 0 to 65°C range, but the military-grade boards extend the temperature range from -40 to 85°C. The military-grade boards will also operate in a condensing-moisture atmosphere. Both grades of boards will tolerate 2G mechanical shocks at a sinusoidal frequency of 500 Hz. The first three boards in the new family will include a CPU, a memory, and an I/O board. The MVME141 CPU boards will supply a 68030 µP and a 68882 floating-point math unit. The MVME224 boards will accommodate as many as 8M bytes of memory, and the MVME326 will furnish a SCSI interface for controlling peripherals. Prices will be published in early 1990; the boards should be available at that time.—Jon Titus

MANUFACTURERS' SPICE MODELS EASE ANALOG DESIGN

Precision Monolithics Inc (Santa Clara, CA, (408) 727-9222) and Harris Semiconductor (Melbourne, FL, (407) 729-4788) now offer Spice models of some of their op amps on floppy disk, thus making it possible for you to simulate analog circuits more accurately. Both companies plan to offer models for most of their linear ICs within a year, and other manufacturers will likely follow suit. PMI's models, although not

perfect matches of actual parts, come much closer to a device's actual performance than those based on the commonly applied Boyle model. PMI currently offers seven models, including ones for the OP-42 fast-settling, OP-64 high-bandwidth, OP-400 quad low-power, and OP-260 current-feedback op amps. PMI's models feature multiple stages, any number of poles and zeros, a JFET- or bipolar-input stage, and no internal grounds. Harris currently provides models for the wideband HA-2539/40; the fast-settling HA-5190; and the low-noise HA-5101/11, 5102/12, and 5104/14 op amps. An applications note containing both the description of the model's architecture and a listing of the model file accompanies each floppy disk.—Anne Watson Swager

TINY $400 COMPUTER RUNS MS-DOS SOFTWARE

No larger than a VCR tape and weighing only one pound, the Portfolio computer from Atari (Sunnyvale, CA, (408) 745-2000) sells for $399.95 and includes a built-in Lotus 1-2-3 file-compatible spreadsheet, word-processing software, a calculator, an appointment book, an address book, and a phone directory. This computer has a standard QWERTY keyboard and runs on three AA-size batteries. The Portfolio's CPU is an 80C88 μP. It comes with 128k bytes of RAM, which is expandable to 640k bytes, and has a card drive that accepts PROM, ROM, and RAM cards for optional software and data storage. You can also order an external card drive that lets your desktop PC access the Portfolio's solid-state memory cards. The Portfolio's internal software is menu driven and can be viewed in frames and overlapping windows via the 40-column × 8-line LCD.—J D Mosley

EXPANSION CHASSIS AVAILABLE FOR MACINTOSH PORTABLE

If you've been looking for an expansion chassis for your Macintosh Portable computer, you can order one from Second Wave (Austin, TX, (512) 343-9661). Dubbed the Expanse Home Base, this unit is a 2-slot 6800 processor-direct-slot (PDS) SE card chassis that attaches to your Macintosh Portable via an interface card and cable assemblies. This $995 chassis contains a 15W power supply, a cooling fan, and two 68000 PDS SE card slots. Measuring 15.5 × 14 in. and tapering in height from 1.5 to 2 in., the Expanse Home Base can be a support platform under your Macintosh Portable.—J D Mosley

LASER PRINTER BREAKS THE $1500 PRICE BARRIER

The HP LaserJet IIP from Hewlett-Packard is a low-end laser printer with a list price of $1495. It produces text with a 300-dpi resolution and prints at four pages/minute. The printer's low cost is mostly due to the incorporation of the relatively small and inexpensive Canon P110 print controller. The controller eliminates paper jams by letting the paper travel only through the front of the printer. In addition, the printer has the flexibility to handle Postscript software.—John Gallant

TEXAS INSTRUMENTS OFFERS FREE ASIC DESIGN KITS

If you are designing a system that will incorporate either the TGC100 series gate arrays or the TSC500 series standard cells from Texas Instruments (Dallas, TX, (800) 232-3200, ext 700), you can request a complimentary design kit, which is valued at $3995. This offer is valid through January 31, 1990. Each design kit contains design, software, and library support plus comprehensive user documentation. These tools provide you with the software and data you'll need to create either a 1-μm CMOS TGC100 gate array or a CMOS TSC500 standard cell.—J D Mosley

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CIRCLE NO 61

PC-BASED ICE FOR Z8 μC FEATURES CONTINUOUS MONITORING

The WICEZ8 in-circuit emulator (ICE) from Wytec Co (Bloomingdale, IL, (312) 894-1440) supports real-time emulation for Zilog Z8 μCs at clock rates as fast as 16 MHz and features a windowed user interface for ease of operation. You use the emulator in conjunction with an IBM PC or a compatible computer, and the vendor supplies PC-based software with the emulator that lets the PC control the ICE hardware. The emulator communicates with the PC over a 38.4k-bps RS-232C link. During emulation, the PC displays a window that lets you continuously monitor 30 memory locations or registers, 17 stack locations, eight breakpoints, and a real-time clock. The $995 emulator provides 32k bytes of emulation RAM, which you can map into your target system in 2k-, 4k-, 8k-, 16k-, or 32k-byte blocks. The WICEZ8's symbolic debugger can use symbol files generated by assemblers from 2500 AD, Microtek, and Zax. Wytec plans to introduce a real-time, trace-buffer option board for the emulator in the near future.—Steven H Leibson

VENDOR REDUCES PRICES OF FLASH MEMORIES

Citing significant increases in volume production, Seeq Technology Inc (San Jose, CA, (408) 432-7400) has reduced the prices of its flash memories—some by more than 50%. The 1M-bit 48F10-200 flash EEPROM now costs $46.75 (100), which is a 54% reduction of the previous $101.20 price. This flash memory now costs twice as much as UV-erasable PROMs; before the price reduction, it was three times as expensive. The price of the 512k-bit 48F512 was reduced 24%, from $37.40 to $26.65 (100). The price reductions affect both the 1M-bit and the 512k-bit flash memories in a variety of packages, from 32-pin plastic and ceramic DIPs to the surface-mount options of LCCs, plastic leaded-chip carriers, and flatpacks.—Julie Anne Schofield

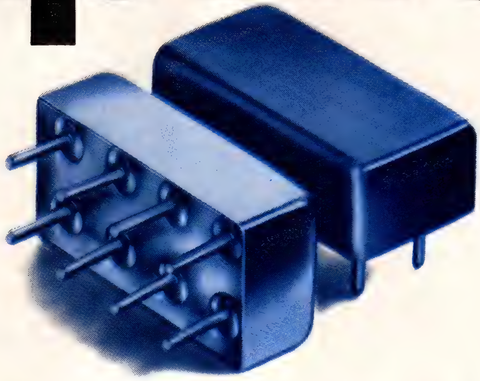
BOARD-LEVEL LOGIC SIMULATOR ELIMINATES BREADBOARDS

PC-board development engineers who have been looking for a digital logic simulator should consider the $995 Schema-SUSIE from Omation (Richardson, TX, (800) 553-9119). Schema-SUSIE (Standard Universal Simulator for Improved Engineering) accepts net lists from the company's Schema II+ schematic-capture program and simulates the configuration for engineering verification. Schema-SUSIE lets you generate test vectors and evaluate your design at the board level or section by section. A waveform generator instantaneously displays the results. Timing analysis reveals design problems at the component level. You can make design changes on-the-fly and then resimulate the whole board or just a section without further compilation.—J D Mosley

POCKET COMPUTER FEATURES C PROGRAMMING LANGUAGE

The PB-2000C pocket computer from Casio Inc (Dover, NJ, (201) 361-5400) integrates the functions of a calculator, a personal data bank, and a personal computer in a small, handheld package. But unlike its predecessors, the PB-2000C employs the C programming language instead of Basic. The $349.95 computer weighs 8.8 oz, runs for at least 25 hours on three lithium batteries, and features a 4-line × 32-column LCD display. The base machine is equipped with 32k bytes of memory, which you can expand to 64k bytes with an optional expansion pack. If C is not your favorite programming language, the company offers optional ROM cards that add Basic and Prolog into the pocket computer's repertoire. Interface modules with Centronics, RS-232C, and floppy-disk interfaces are also available.—Steven H Leibson

rugged plug-in amplifiers



0.5 to 1000MHz from $13.95 (10 to 24 qty)

Tough enough to meet full MIL-specs, capable of operating over a wide -55° to +100°C temperature range, in a rugged package...that's Mini-Circuits' new MAN-amplifier series. The MAN-amplifier's tiny package (only 0.4 by 0.8 by 0.25 in.) requires about the same pc board area as a TO-8 and can take tougher punishment with leads that won't break off. Models are unconditionally stable and available covering frequency ranges 0.5 to 1000MHz, NF as low as 2.8dB, and power output as high as +15dBm. Prices start at only $13.95, *including* screening, thermal shock -55°C to +100C, fine and gross leak, and burn-in for 96 hours at 100°C under normal operating voltage and current.

Internally the MAN amplifiers consist of two stages, including coupling capacitors. A designer's delight, with all components self-contained. Just connect to a dc supply voltage and you are ready to go.

The new MAN-amplifiers series...
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MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	GAIN dB flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB †ldB Gain Compression ◇Case Height 0.3 In.
Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

*Active Directivity (difference between reverse and forward gain) 30 dB typ.

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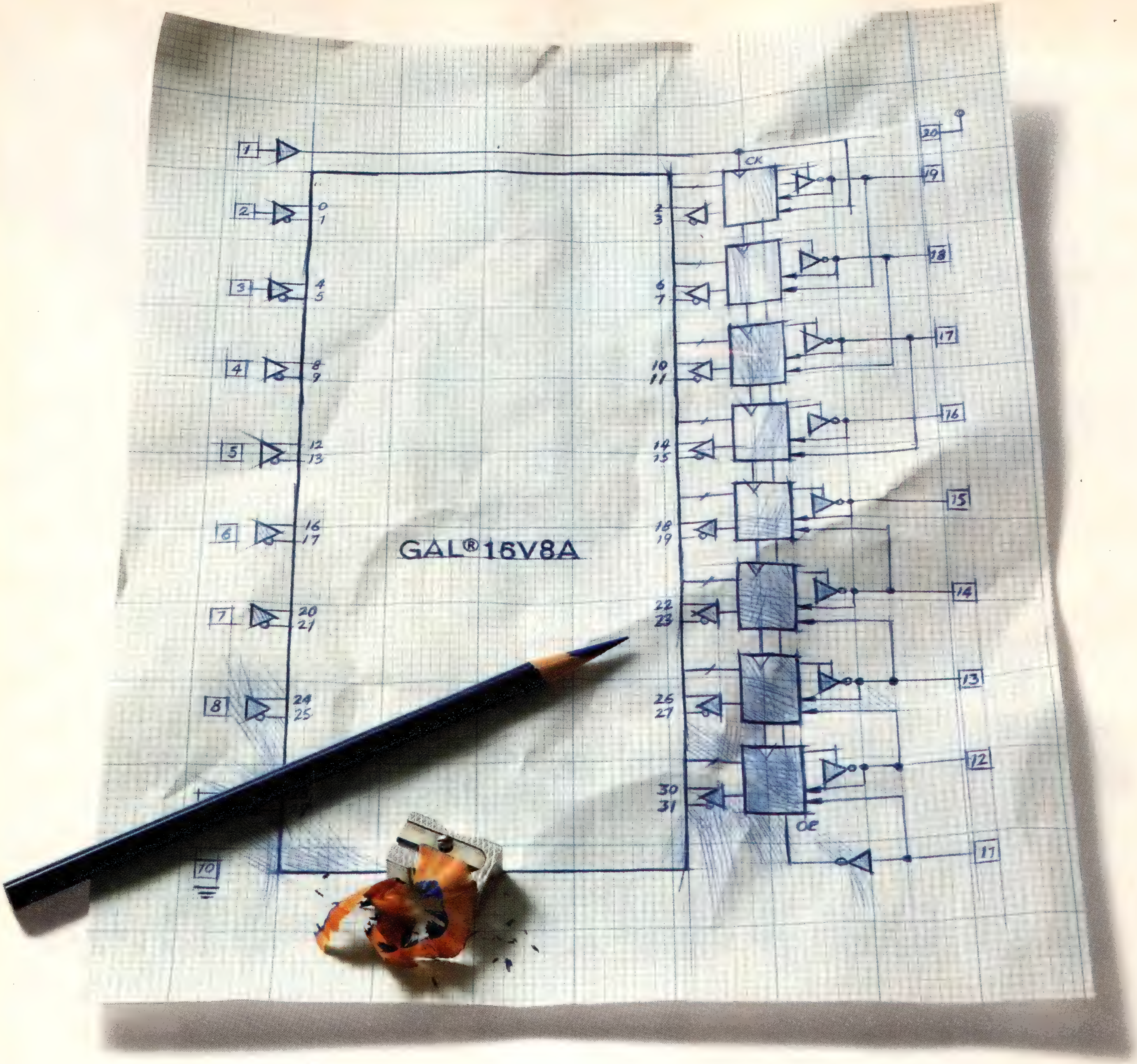
CIRCLE NO 62

C118 REV. E


low pass
HIGH PASS
low pass
HIGH PASS



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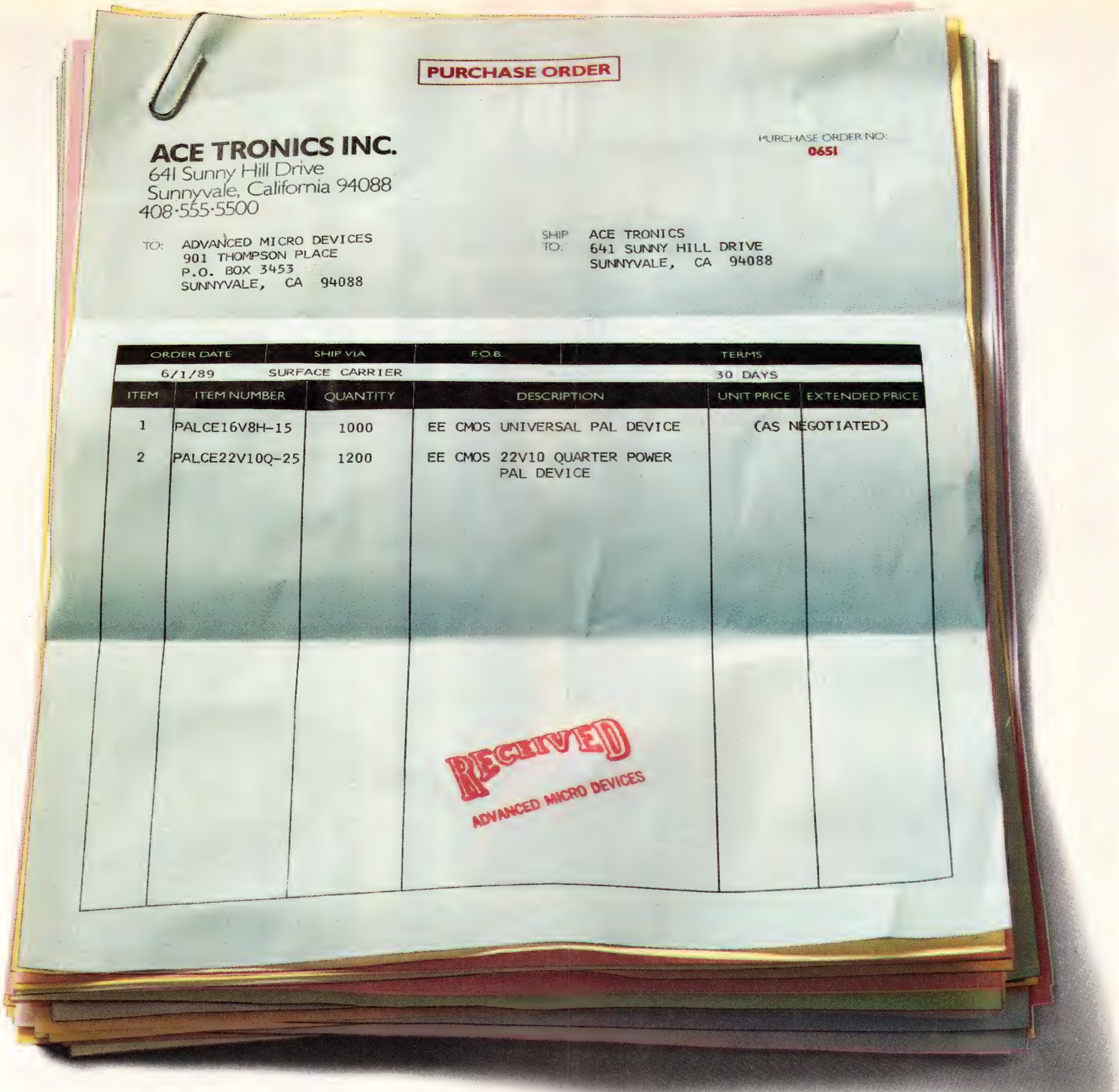

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CIRCLE NO 65

Distinguishing part numbers and functions

In my article (EDN, September 28, 1989, pg 145), I mentioned that not all digital ICs from different families that have similar part numbers are *functionally* similar. Here is a preliminary list of digital ICs that do not have the same pinout as other ICs of the same nominal number. (The list took me a full hour to compile after studying a full set of National Semiconductor digital, TTL, and CMOS databooks, as well as Texas Instruments and Motorola databooks. Heck, it probably took three hours. It may not be a perfect list, but it's the best I have ever seen—heck, it's the *only* one I've ever seen—and it cuts out a lot of baloney and malarkey.) For example, the MM74C86 and the DM74L86 both have the same pinout, but it is not the same as the pinout of the 7486, 74S86, 74LS86, 74HC86, and the 74C386.

"THE CHIEF HONCHO IN ENGINEERING WANTS US TO D-I-S-A-S-S-E-M-B-L-E THE R-O-B-O-T."

The following list of parts all share the same pinout: 74H01; 74L51, LS51; 74H53; 74L54, LS54, H54; 74H55; 74L71; 74l78, LS78A; 74L85, C85; 74L86, C86; 74L95, C95.

That's all I can find right now. Perhaps readers might also want to be aware that a 74107 is pulse triggered, but the 74LS107A is edge triggered, so in some cases they may act interchangeably, and in others, not quite the same.

Robert A Pease
Staff Scientist
National Semiconductor
Santa Clara, CA

He votes for full HDTV

Norman Hill's letter on HDTV (EDN, June 22, 1989, pg 46) was right on, but I want to expand just a small pixel.

We are already stuck with an inferior system because the FCC forced compatibility back when we went from black and white to color.

The European formats, PAL and SECAM, present superior color video. We had to wait behind the rest of the world for stereo TV because those same powers argued over the method while both Europe and the Far East were already enjoying it.

I vote for full HDTV. And forget about compatibility. "Go for the Gold!"

Actually, we already know that many manufacturers have monitors and televisions on the market now that are "multiscan" (scan as necessary to suit the signal coming in). I now own a Sony that plays both NTSC and PAL, and it even switches automatically. So being able to receive HDTV and the current system is not a problem.

Eugene B Simmons Jr
Harvest, AL

He'd like a "pin-counting" aid

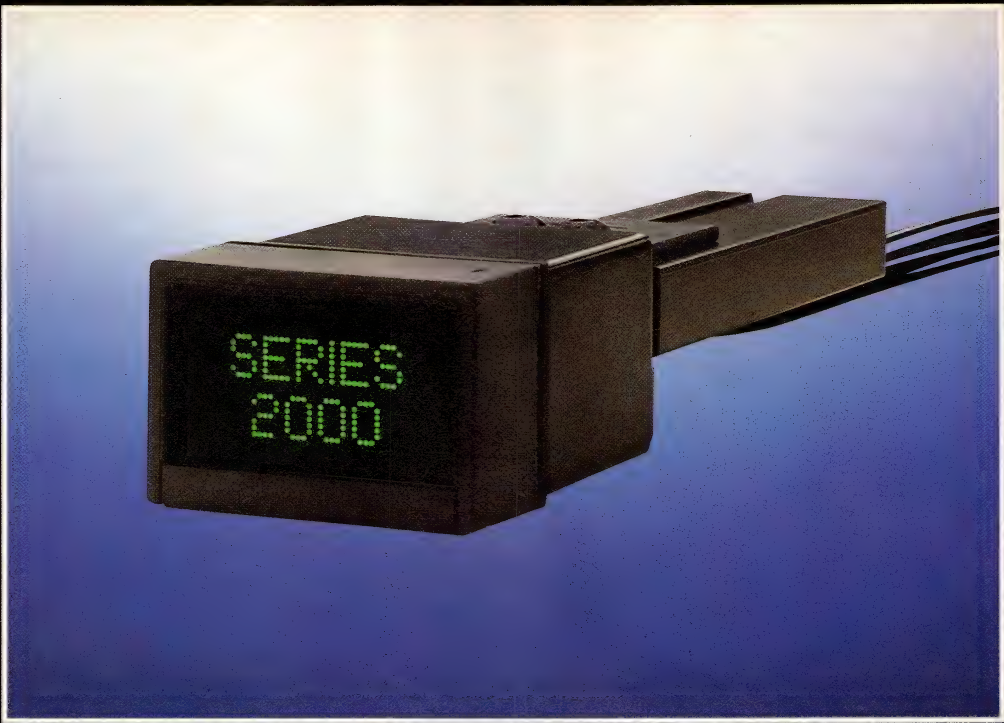
In the past years I've been designing with larger and more complex ICs. One particular area that has consumed a lot of my engineering time has been the counting of pins on 40-pin and PLCC (plastic leaded chip carrier) packages. For years I've been thinking that the industry knew about this and considered it a problem that would some day be addressed. Because I have not yet seen a solution to this problem, I'd like the industry to consider a possible fix that I feel would not cost a great deal, and that would add value to sockets for PLCC ICs and to PLCC chips themselves.

The idea is to simply add "pin marks" every fifth or tenth pin from left to right on PLCC sockets, if you are a socket manufacturer, or on PLCC packages, if you are an IC fabricator. The implementation on sockets would take place at the same time that pin 1 is marked, meaning minor changes to the injection mold. The implementation for PLCC ICs would take place during the labeling of the part or preferably during the molding of the PLCC case. The latter would be a more permanent method.

Luis Taveras
President and Production Manager
GMM Research Corp
Santa Ana, CA

Price correction

In Table 6, entitled Representative EEPROMs (EDN Special Report, September 1, 1989, pg 110), the price for the XL93C46 reads \$0.36 (100); the correct price for the XL93C46 is \$1.36 (100).



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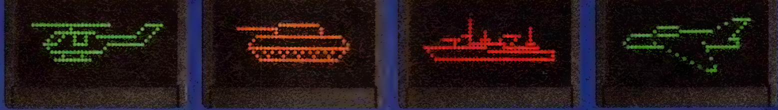

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Repetitive Bandwidth	1 GHz		1 GHz		
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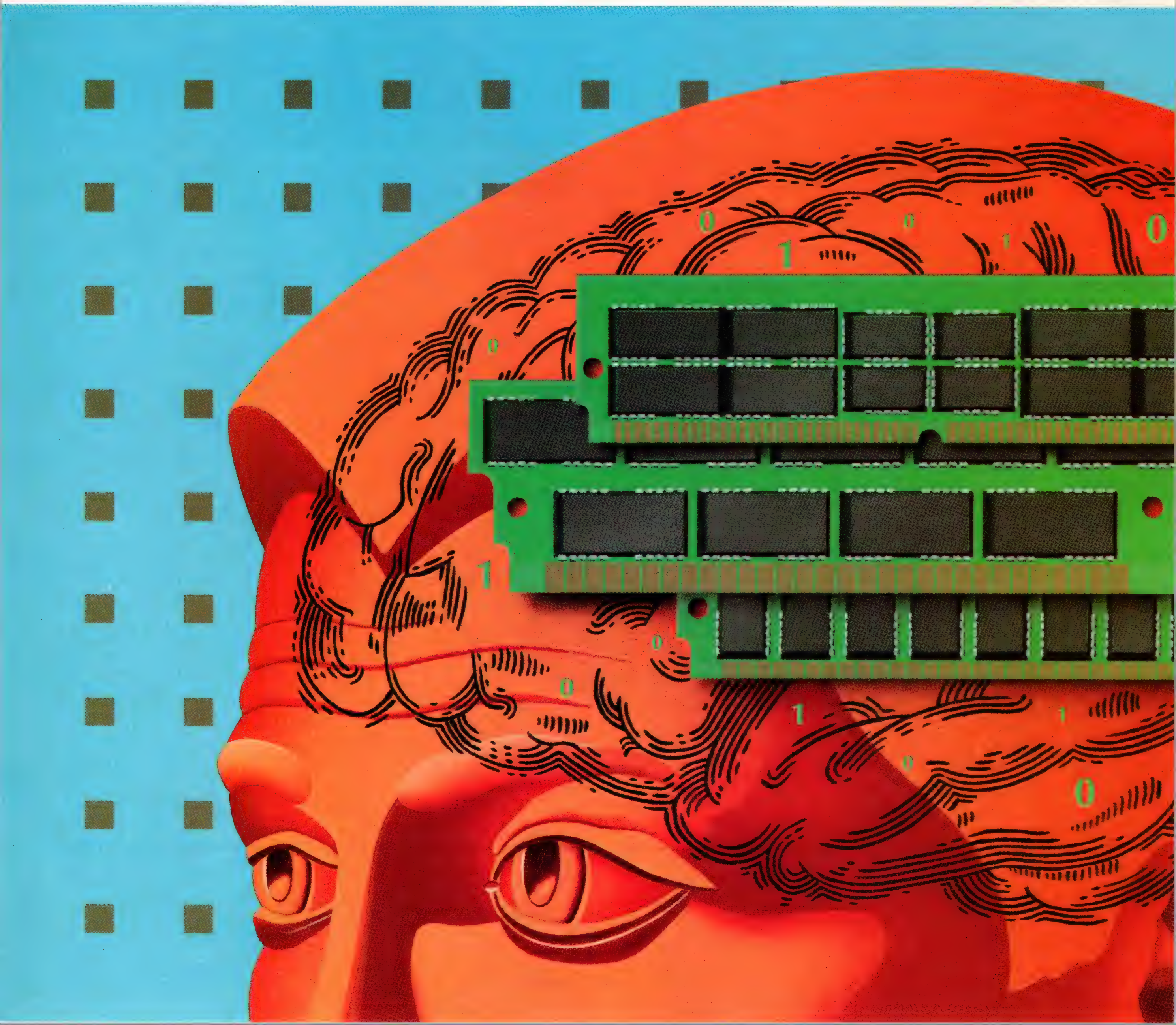

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		Package	
Organization	Speeds	Outline	Pinout
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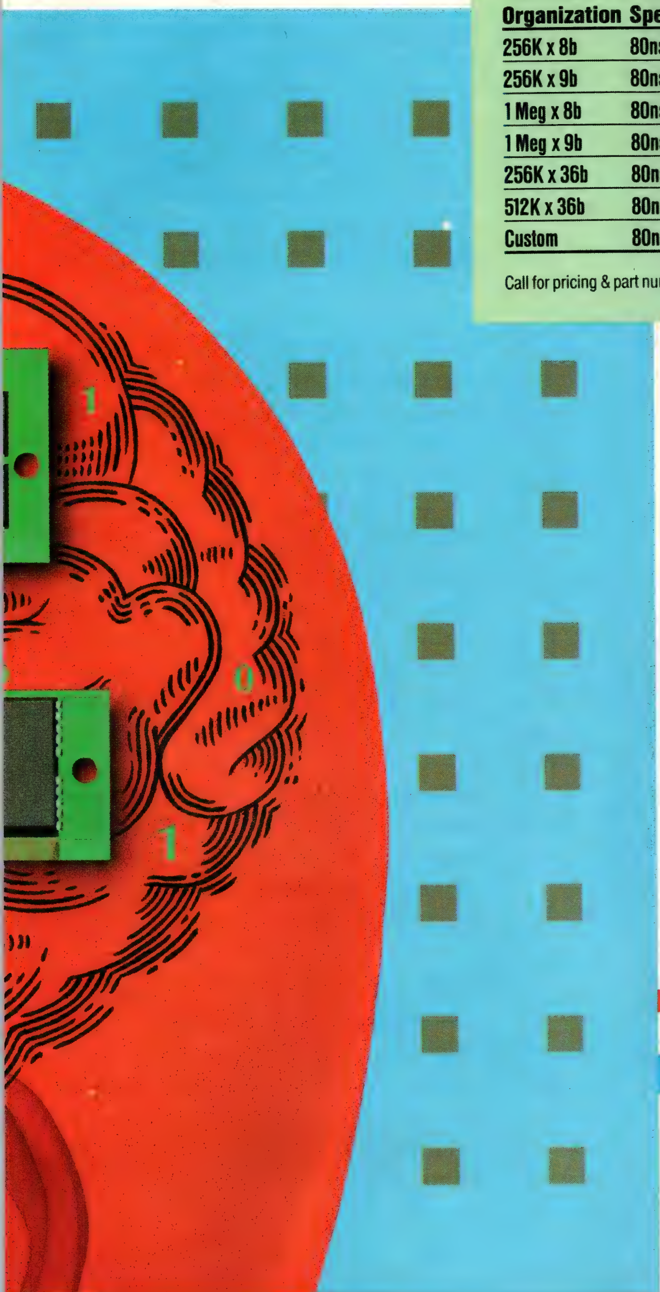
256K x 9b	80ns, 100ns, 120ns	JEDEC	JEDEC
1 Meg x 8b	80ns, 100ns, 120ns	JEDEC	JEDEC
1 Meg x 9b	80ns, 100ns, 120ns	JEDEC	JEDEC
256K x 36b	80ns, 100ns, 120ns	JEDEC	Custom
512K x 36b	80ns, 100ns, 120ns	JEDEC	Custom
Custom	80ns, 100ns, 120ns	Custom	Custom

Call for pricing & part numbers



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1989 Linear Applications Seminar, Bellevue, WA. Various locations and dates. National Semiconductor, Box 58090, Santa Clara, CA 95052. (800) 548-4529. Through December 1.

System Application Architecture (SAA) World (conference and exhibition), Chicago, IL. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3880. FAX 508-470-0526. October 30 to November 1.

Digital Signal Processing, Single-Chip DSP Processors, Development Systems—Theory, Design, and Applications, London, UK. In the US, Dr Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. FAX 617-969-6689. In the UK, Mr Andrew Christofi, Loughborough Sound Images, Loughborough, UK. (44) 509-231-843. October 30 to November 2.

Unix Expo '89, New York, NY. National Expositions Co, 15 W 39th St, New York, NY 10018. (212) 391-9111. FAX 212-819-0755. November 1 to 3.

Distributed Data Base Environment: Present and Future (seminar), New York, NY. Technology Transfer Institute, 741 Tenth St, Santa Monica, CA 90402. (213) 394-8305. FAX 213-451-2104. November 2.

1989 DOD-STD 2167A/2168 Seminar, San Diego, CA. David Maibor Associates Inc, Box 846, Needham Heights, MA 02194. (617) 449-6554. November 2 to 3.

SMT Equipment Comparison, Evaluation, and Selection (short course), Bethlehem, PA. John Gilda, National Training Center For Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18017.

CALENDAR

(215) 861-5450. FAX 215-861-5373. November 2 to 3.

Visual Communications and Image Processing '89, Philadelphia, PA. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. November 5 to 10.

OEM Europe '89, Paris, France. Bureau International de Relations Publiques, Freddy J Rodriguez, 25 rue d'Astorg, 75008 Paris, France. (331) 47-42-20-21. FAX 331-47-42-75-68. November 7 to 10.

Productronica '89 Munich, West Germany. Gerald Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. November 7 to 11.

Fallcon '89 Cedar Rapids, IA. Fallcon '89, Box 451, Marion, IA 52302. (319) 396-7924. November 8 to 9.

Training Workshop for Visual Inspection of ICs and Hybrids, Boston, MA. Integrated Circuit Engineering Corp, 15022 N 75th St, Scottsdale, AZ 85260. (602) 998-9780. FAX 602-948-1925. November 9 to 10.

Supercomputing '89, Reno, NV. Lyz Dunham, NASA Ames Research Center, Moffett Field, CA 94035. (415) 694-4370. November 13 to 17.

Wescon/89, San Francisco, CA. Wescon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. FAX 213-641-5117. November 14 to 16.

VMEbus in Industry, Paris, France. VMEbus International Trade Association, Box 192, NL-5300 AD Zaltbommel, The Netherlands. 31-4180-14661. FAX 31-4180-15115. November 21 to 22.

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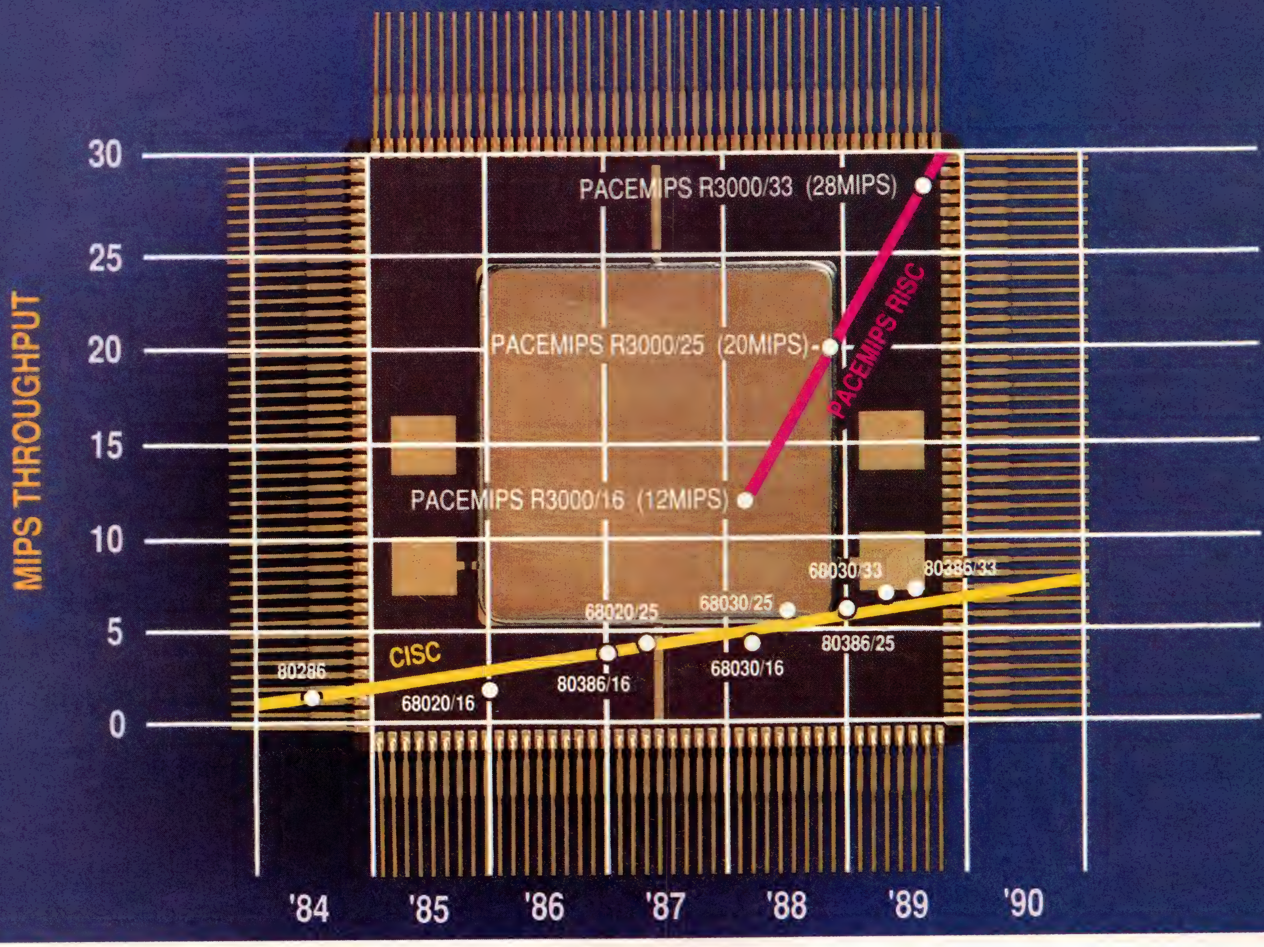

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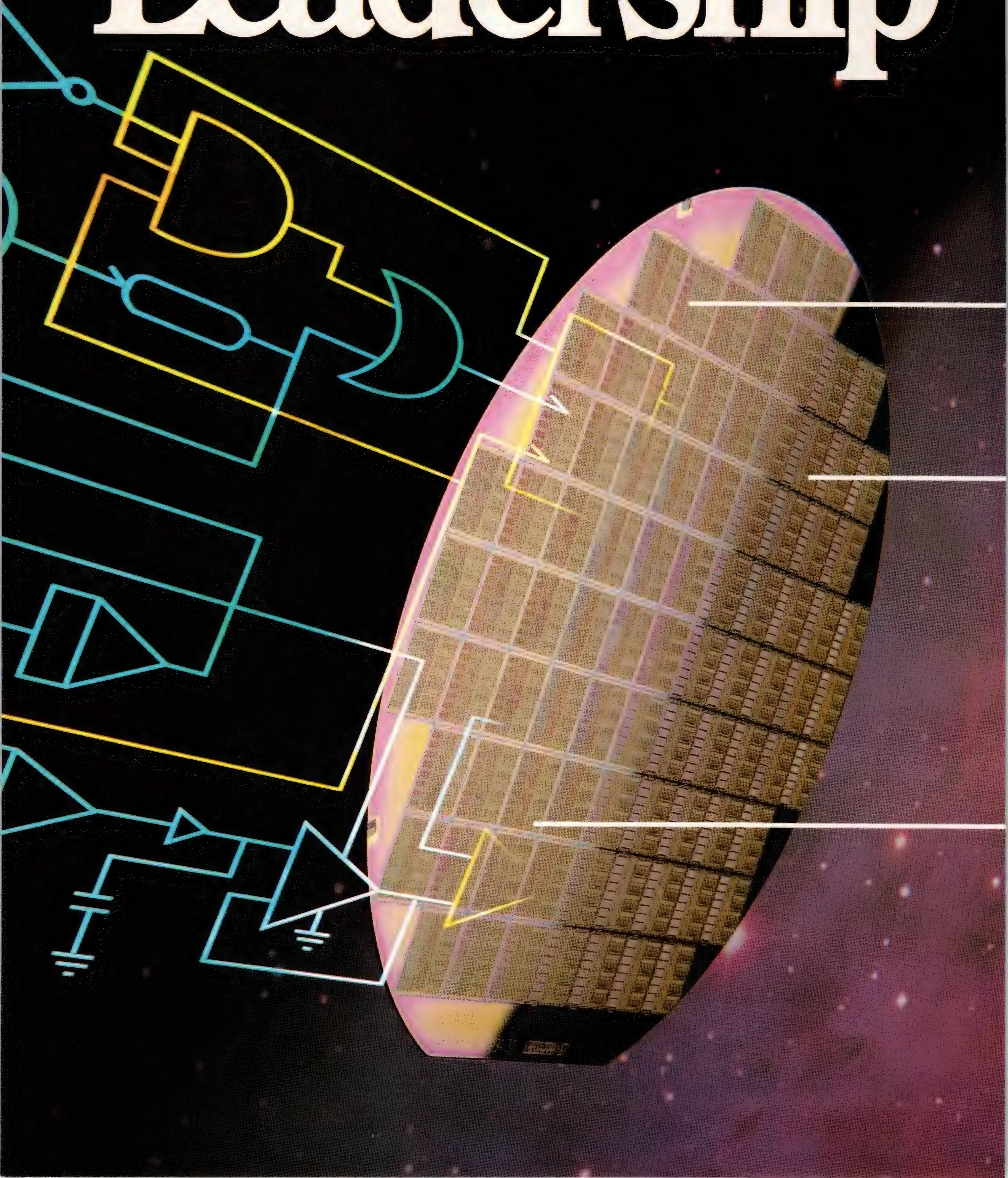

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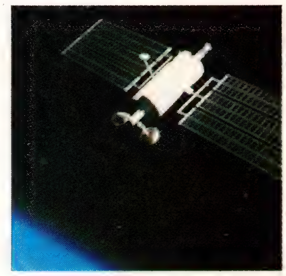

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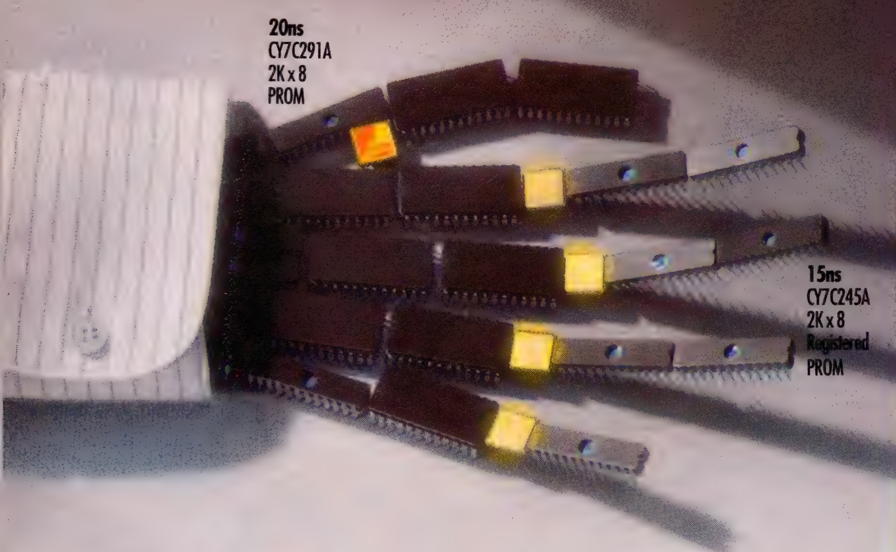

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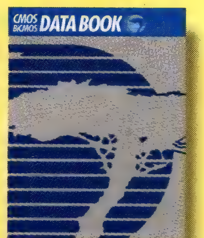

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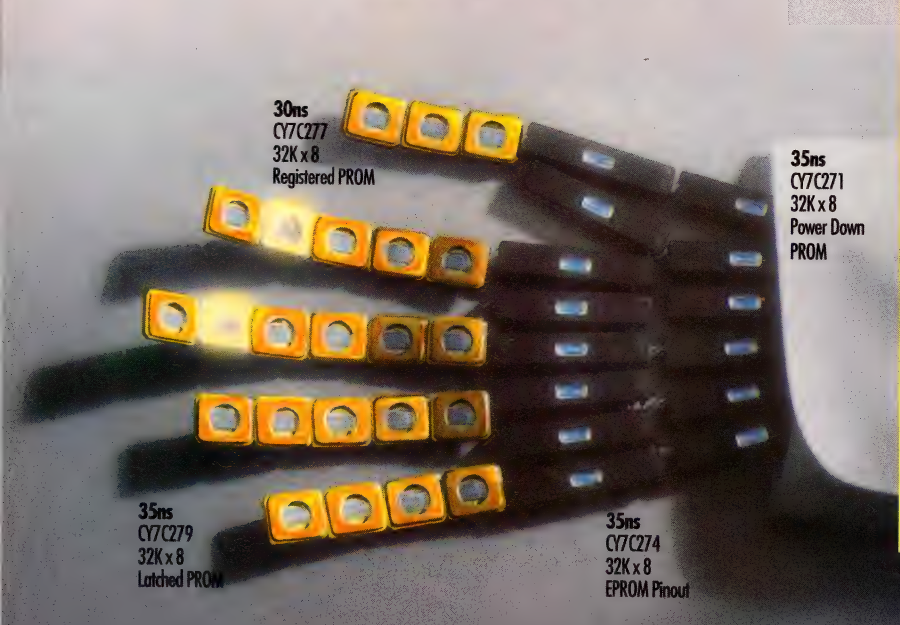

EDITORIAL

Rules to live by

I'll be frank. As an American, I'd have difficulty adapting to the Japanese way of life. There's too much conformity for my independent spirit and too much polite obliqueness for my straight-ahead style. When I recently returned from a two-week stay in Japan, I was glad to be back in the good old USA.

But please understand this: Although I don't like Japanese rules for living, it's not for me to judge those rules, because I don't have to live by them. If Japanese rules work for the Japanese, then who am I to complain?

In the article beginning on page 59, I report the observations of several American engineers who have lived and worked in Japan. Some of the Americans' comments about the Japanese workplace seem harsh, and yet all the engineers I interviewed for the article viewed their time in Japan as a positive experience. Their candid observations are just that—observations. If they seem harsh when you read them, it could be because you're judging them by American rules—rules that don't apply.

According to American rules, the Japanese workplace seems rigidly structured, but this rigid structure furnishes unambiguous goals and unambiguous plans for reaching those goals. I have yet to see a Japanese engineer working without a clear sense of purpose.

Workdays in Japan are depressingly long by American standards, but the Japanese take enormous pride in what they accomplish in those long days.

Business negotiations and even personal communication in Japan can be exasperatingly indirect, because Japanese culture stresses politeness and avoidance of conflict. But if you're frustrated by overextended politeness, at least you'll never be snarled at by a rude Japanese cab driver.

I could go on and on. I could mention the inferior treatment of women in the Japanese workplace, but American women were treated equally badly not too many years ago and still haven't achieved equality. I could mention the Japanese obsession with education and careers at the expense of joyful living, but it only conjures up visions of America in the 1950s.

Finally, I could mention unfair trade. I could mention, for example, how "Japan Inc" competes unfairly with American companies through a cooperative effort of Japanese industry and government. But such cooperation isn't at all unfair according to Japanese rules. In fact, many Japanese wonder why there isn't similar cooperation in the US. For that matter, many Americans wonder the same thing.

I don't mean to make light of the trade situation. The Japanese do invoke practices that, by rules familiar to Americans, are simply unfair. A key point to remember, though, is that they're playing with a different set of rules—rules that might seem strange to us, but perfectly sensible to them. Before we judge their behavior, whether in the engineering lab or in the international arena, we have to agree on what the rules should be. They might have to adopt some of our rules, and we might have to adopt some of theirs, but only when we agree to follow the *same* rules can we begin to judge each other.

Gary Legg
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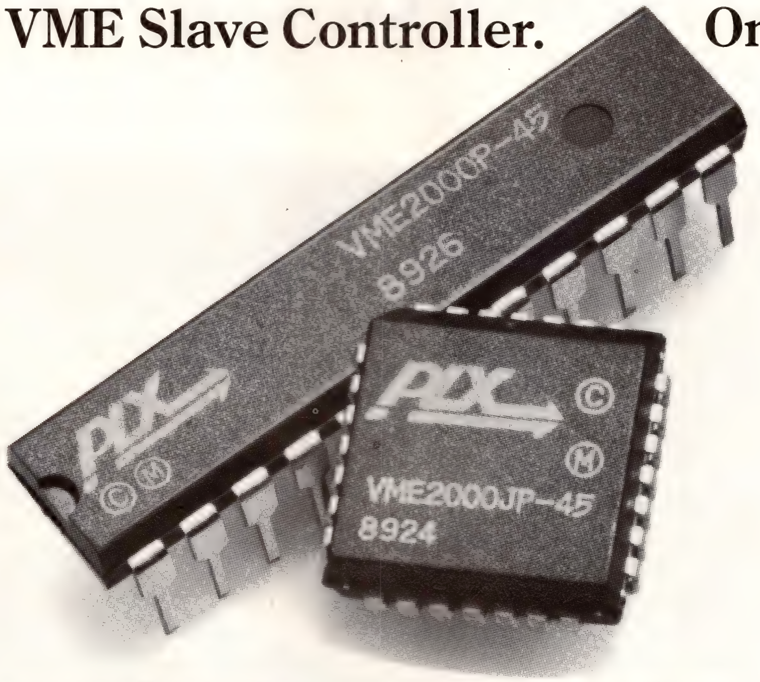

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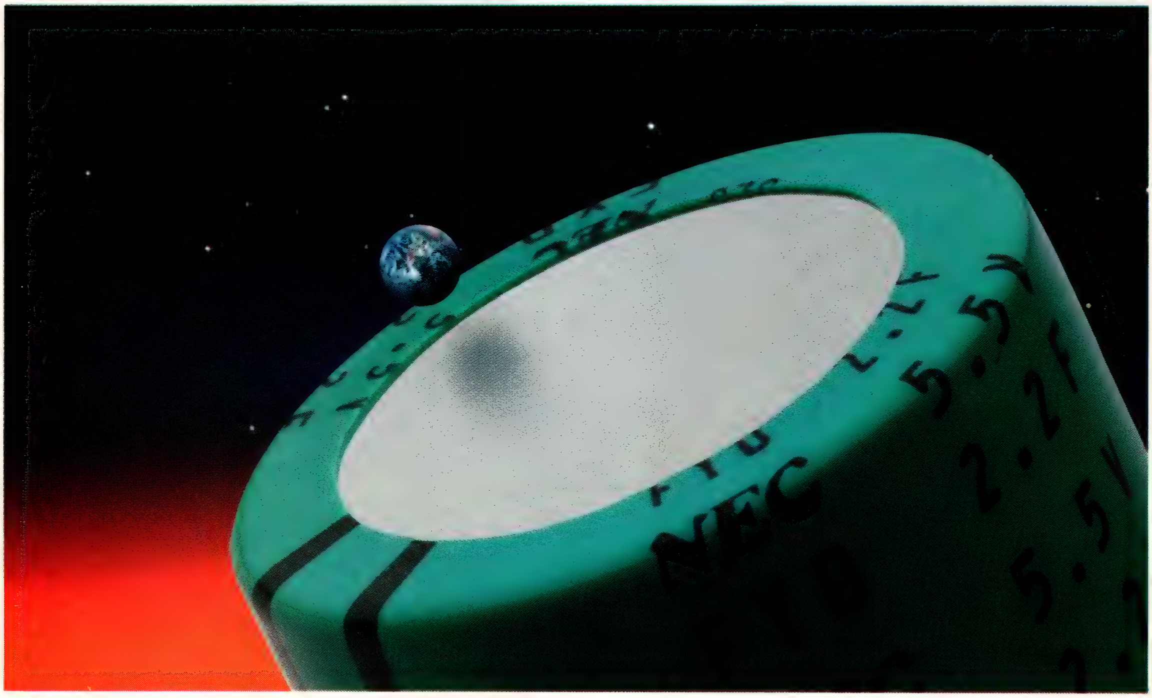

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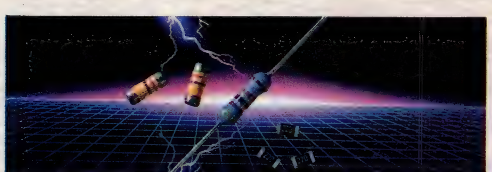
ENTERING THE HIGH-TECH STAGE: TAIWAN

It certainly takes more than seven days and a good investment climate to transform an agricultural society into the world's 12th largest industrial nation. The Republic of China's meteoric rise in the international community of economic hardplayers over the past 40 years is based on several contributing factors, but first and foremost are the Taiwanese people and their work ethics, their diligence and absolute will to succeed in today's increasingly competitive markets. Taiwan is no longer a place for cheap contract manufacturing. The times when the R.O.C. was Paradise Island for those seeking low labor costs and mediocre product quality definitely belong of the past.

PROPER PLANNING MADE IT HAPPEN

The educational infrastructure on the island has become one of the best in Asia. Providing high-level mass education has been a major task which the R.O.C. government has successfully mastered. Today, Taiwan is not only boasting a skillful and motivated blue collar workforce but also a large pool of white collar employees, many of whom hold higher academic degrees from universities abroad. Every year, graduates from more than 100 colleges and universities turn to Europe and the U.S. to complete their training, mainly in high-technology fields. Consequently, Taiwan is now in a process of transition from an OEM (original equipment manufacturing) based economy to one which is also rooted in original design manufacturing (ODM). As recently as 1985, only 5 per cent of Taiwan's Electronic Industry (the island's No. 1 industry) products were sold under their own brand names. By 1988, that figure increased to more than 20 per cent and it's on the rise, especially in the field of PC's, where almost 40 per cent brand name marketing is the current rule. Still, OEM will remain an important economic factor.



ECONOMIC POLICY ADJUSTMENTS

Taiwan's "economic miracle" resulted in a gross national product of nearly $19 billion in 1988, maintaining the average economic growth of 7 per cent. 1988's per capita income of $ 6045 was among the highest in Asia. Since martial law was lifted, there have been tremendous changes in the R.O.C.'s economic policy. To improve trade relations and attract investors, tariffs and duties on some 3000 imported industrial products have been slashed; for several high-tech products such as IC's, the tariffs are as low as 1 per cent. The biggest problem Taiwan's export oriented industries are currently facing is the steady appreciation of the currency. The New Taiwan Dollar had been artificially kept at an exchange rate of 40 to the U.S. dollar for years. As the country accumulated more and more foreign currency reserves-in fact Taiwan has the world's largest per capita reserves this year-there was a need to bring the NT$ exchange rate to a more realistic level. Under international pressure, especially from the U.S., the currency was put on a free floating base in 1985. Since then, the Taiwan dollar has appreciated some 40 per cent against the greenback; this year's average exchange rate is as low as 25:1. Still, this is not the end to international discontent. It seems like Taiwan will have to let its currency float to its true value. The U.S. is especially dissatisfied, since it has suffered from Taiwan's trade surplus several years already. Even though a significant portion of the island's exports to the U.S. is in fact re-exports (products assembled by American owned companies for American markets) the trade imbalance is causing serious economic friction between these two long-time partners. The tariff reforms have already helped to decrease the surplus to $10 billion, 40 per cent down from $19 billion in 1987. "Buy American" campaigns pushed Taiwanese per capita purchases of American goods up to $650 in 1988. However, Taiwan's investment climate remains quite attractive. Highly trained manpower and the government's current R&D-dedicated policy

bring more and more foreign high-tech companies to the island. Investments in wholly owned subsidiaries, factories, research laboratories and joint-ventures are increasing, despite rising labor costs, especially since infringements on patents and copy rights are strictly prosecuted by official investigators. And while assemblers are moving to offshore production sites such as Thailand and Mainland China, High-Tech moves into the R.O.C....

COMING A LONG WAY - TAIWAN'S ELECTRONIC INDUSTRY

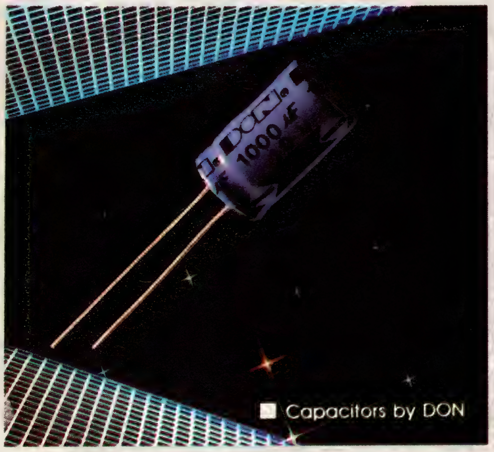
It all began with consumer electronics. Back in the sixties, when Taiwan labor was cheap and margins for low-end products were high. Times have changed and so has the level of industrial production. Eventhough electronic data processing devices ousted them from rank 1, consumer electronics still make about 30% of Taiwan's Electronic Industry's output.

Over the past ten years, the industry's trend clearly shifted from cheap mass production toward higher value added products. In 1988, Taiwan supplied 25 percent of the world's personal computer market and almost 30 percent of all IBM compatibles. The production of high-end components such as semiconductors and ICs rose sharply. This looks fine on paper, yet the electronic industry is facing some major problems:

well established manufacturer of high-end capacitors with branches in Korea and Honkong, is prepared to produce electrolytic capacitors in Indonesia.

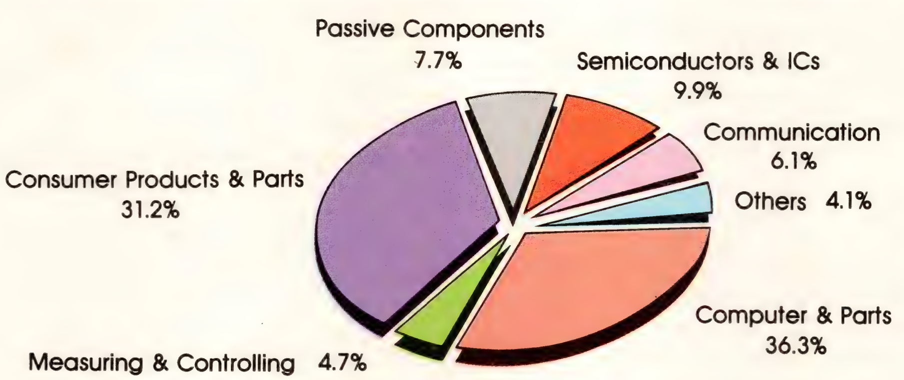
Other manufacturers decided to meet the labor shortage/labor cost problem by investing in factory automation.

Says Alex Hsieh, president of TEC Taicera, Taiwan's foremost hermetic IC assembly house which acquired the U.S. coporation GTE in 1988: "Factory automation and computer integrated manufacturing (CIM) are long term solutions. If there aren't enough workers, machines are needed to take their place."



■ Capacitors by DON

The R.O.C. government is supporting automation to defuse labor shortages and hopes that a profitable automation equipment supply industry can be established. Government institutions such as ERSO (Electronic Research & Service Organisation) are sponsoring R&D activities regarding CIM.



Electronic Industry's Export Production in 1988

The sales of value-added products aren't too promising. Rising labor costs and a strong appreciation of the currency make Taiwan a less attractive place for low-end production. Since 1985 monthly labor costs have doubled from $300.48 in1985 to $602.84. As the industry will also face a severe lack of skilled labor in the near future, some farsighted companies already moved production sites to other South-East Asian countries such as Thailand or Malaysia. Some investments also went into mainland China. DON, an extremely

Since Taiwan still lacks technologies that can really influence international markets, production flexibility has to be maintained. Many of the hundreds of back-alley manufacturers already vanished from the scene, the future obviously belongs to more well-heeled companies. While smaller enterprises seek niche products, industrial leaders try to build strength in value-added mass production.

Yet the move to broader and more sophisticated product ranges is hindered by severe shortages of key components such as

DRAM, which are not only essential for computers but also for advancing semiconductor technology. According to spokespeople of the electronic industry, Taiwan-made DRAM will be a determining factor for the island's future role in international markets. Currently, there are four DRAM fabrication projects, all of which are supported by government institutions.

Import and Export Value in 1989

Products	Export	Import
Computer	4,762.4	2,217.9
Consumer Products	2,879.0	445.4
Telecommunication	637.7	229.4
Measure & Control Equipment	299.4	242.7
Electronic Components	1,046.8	799.1
Semiconductors & ICs	1,345.5	2,217.9
Consumer Electronic Parts	1,365.1	666.5
Displays & Tubes	529.3	1,165.8
Total	13.613.3	7,309.0

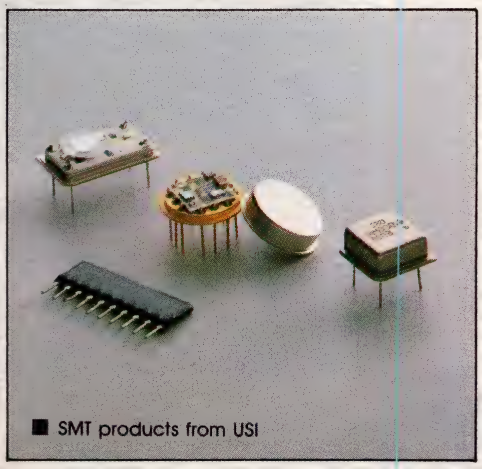
Value in million US$
Source: Council for Economic Planning and Development

■ DOM's fabrication hall

Another serious lack can be seen in the field of optical devices. Except for Taiwan's leading scanner manufacturer, Mikrotek, which is also specialising in CNC products and MICE (Micro In Circuit Emulators), most of the companies suffer from a lack of mechanical and optical skills. It seems to be very unlikely that there'll be a stronger orientation toward optical-related production in the near future.

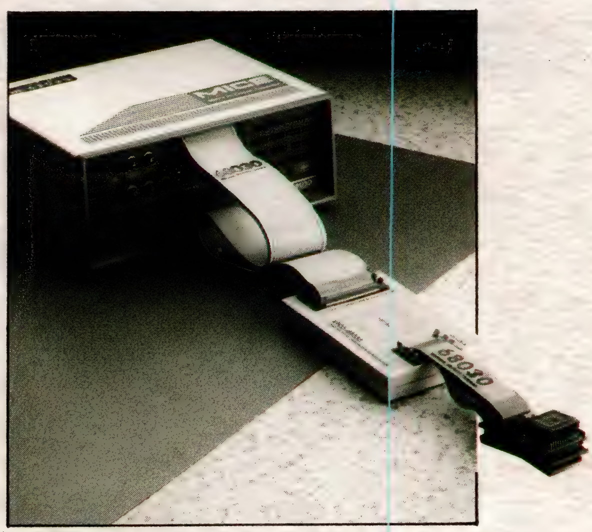
■ Computer Integrated Manufacturing at [illegible]

Despite the fact that Taiwan is still importing twice as many semiconductors and integrated circuits as there are exported, this part of the electronic industry is doing extemely well. Growth rates around 35 percent have been the rule for the last years, due to the growing trend to implement SMT (Surface Mounting Technology) "SMT products are an absolute must for those who want to make it into the next decade." says Ching An Shih of USI, an internationally rewarded maker of Oscillators and Hybrids. He continues: "We didn't recieve the Q1 Preferred Quality Award from Ford in 1988 because we're nice people. We keep investing in R&D and quality control and that's how you keep pace with growing demands."

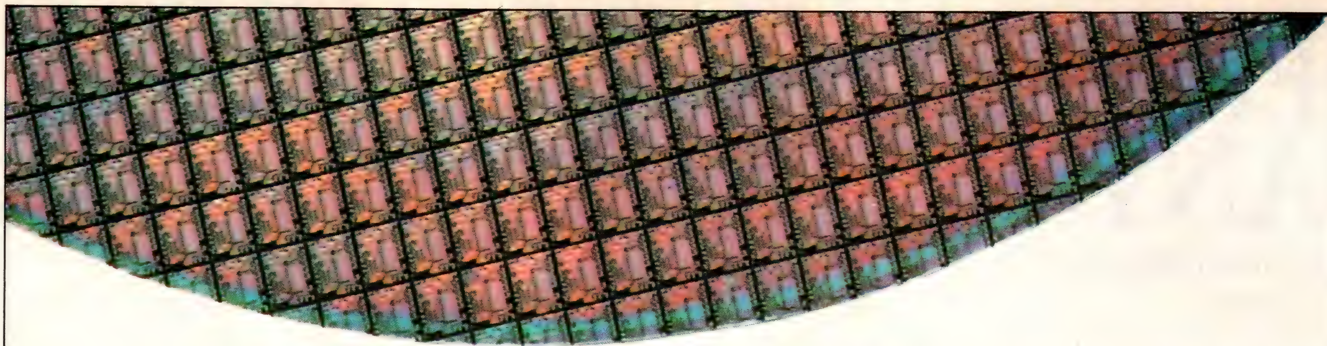


■ SMT products from USI

Currently, the electronic industry is quite concerned about European markets. While the U.S. is still the strongest export market for Taiwanese electronic products - some 42 percent of 1988's total exports were chan - neled into the U.S.A. in 1988 - companies rush to establish branch offices, service centers and warehouses in Europe before the announced market unification in 1992.



Though suffering somewhat from a lack of corporate vision, most of the companies are confident that production flexibility and versatile engineering skills will lead them safely to future success.



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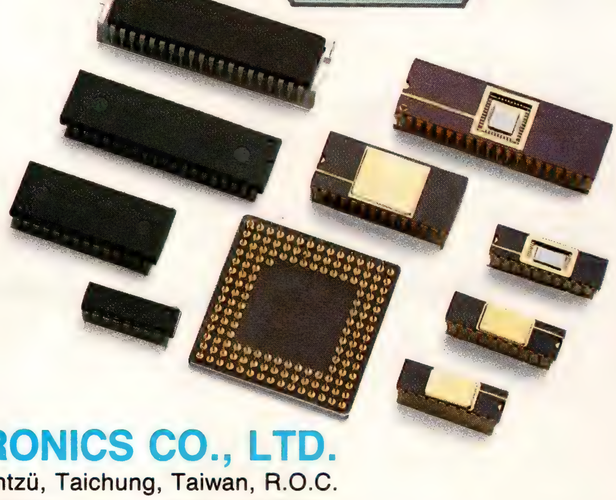

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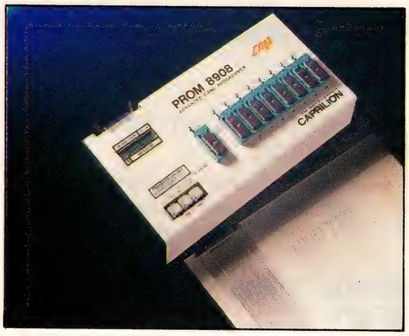

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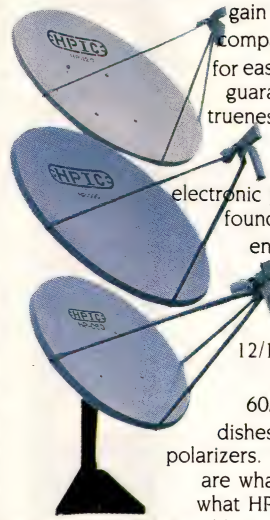

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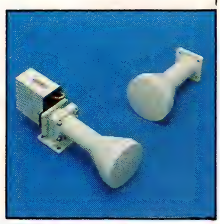

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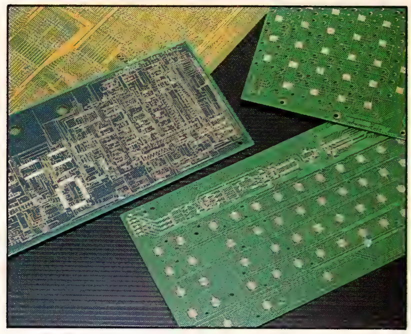

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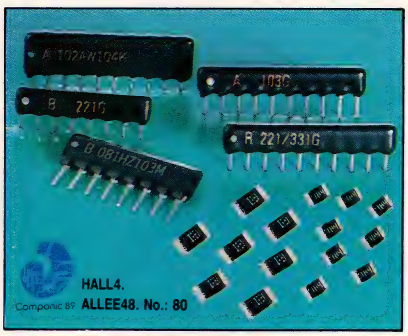

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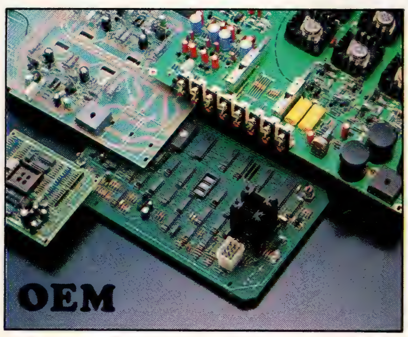

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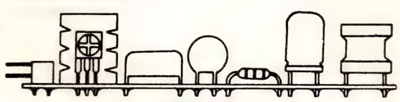

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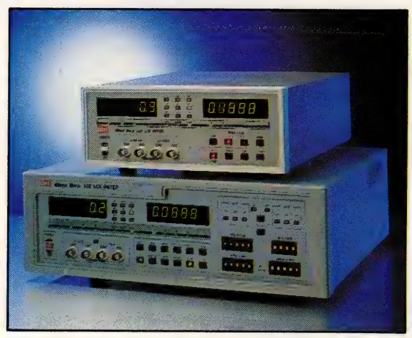

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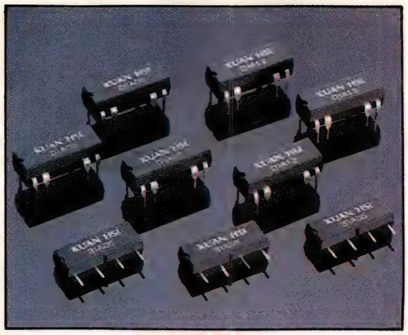

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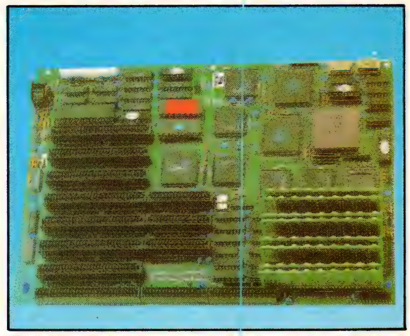

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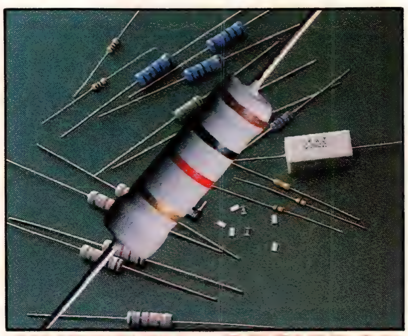

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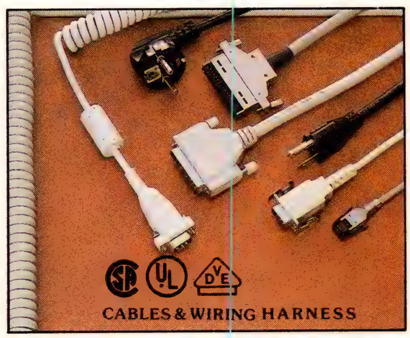

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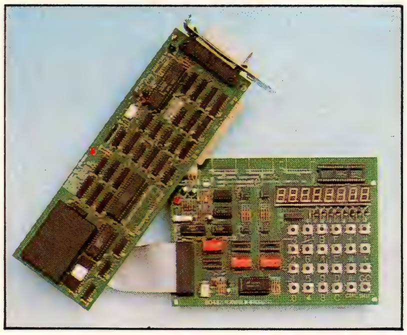

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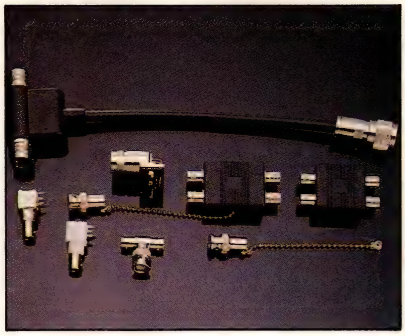

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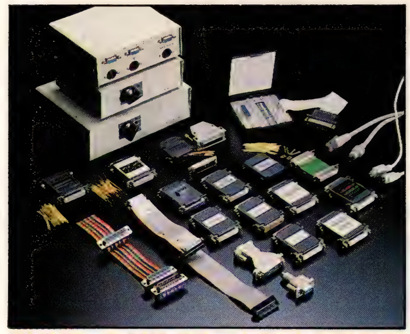

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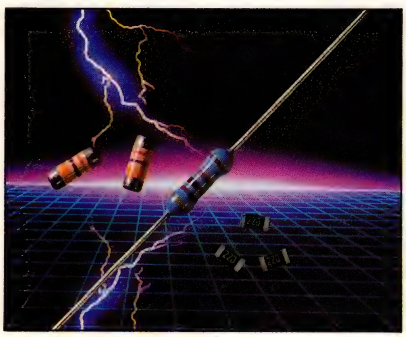

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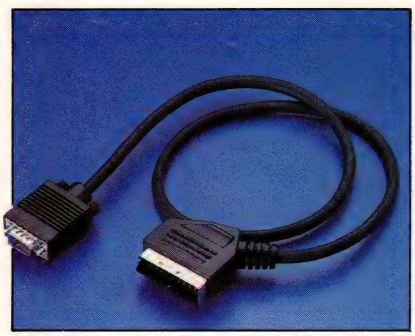

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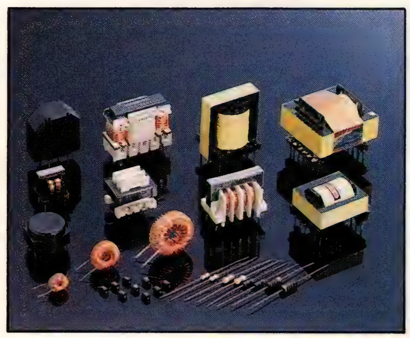

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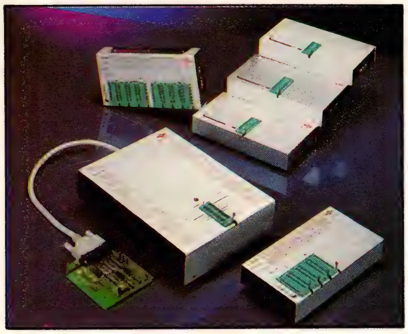

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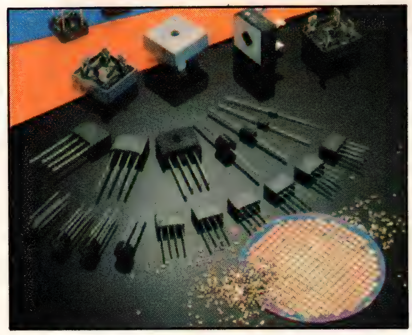

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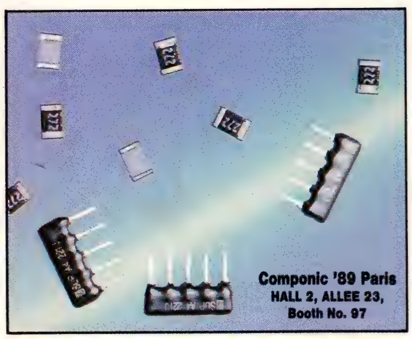

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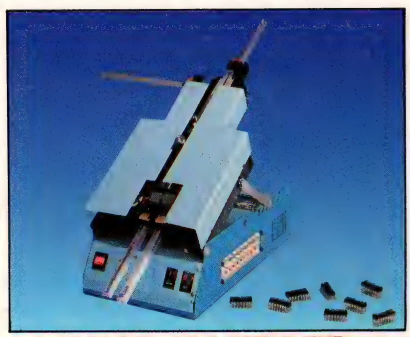

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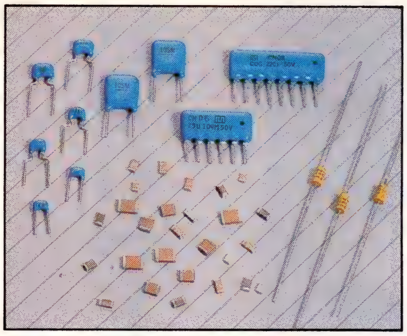

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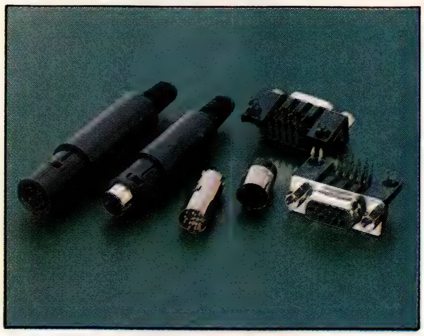

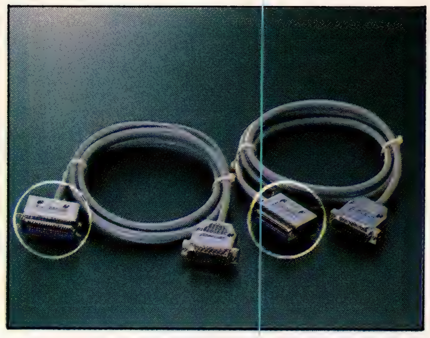

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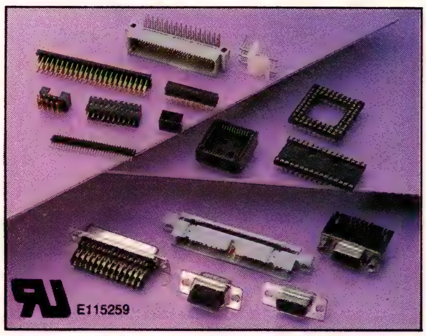

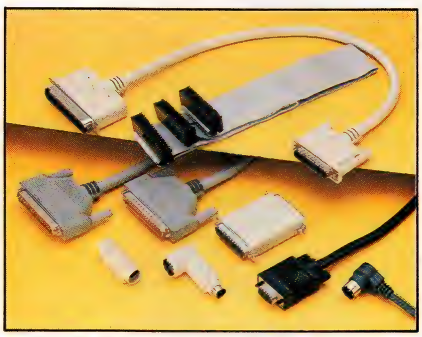

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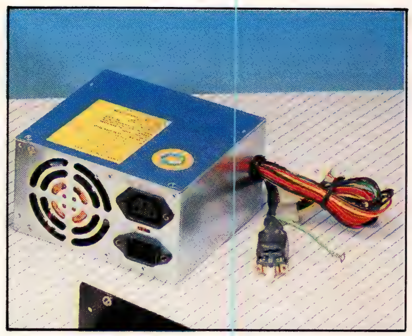

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CIRCLE NO 176

CIRCLE NO 177

inside ASIA

American engineers in Japan:

Same profession, different world

Article and photographs by
Gary Legg, Special Projects Editor

日本

No matter what she does in the plant where she works or in the town where she lives, Tektronix engineer Karen Keough stands apart from the crowd. It isn't simply because she's a good engineer, or that she works in a male-dominated field. Mostly, she stands apart from her crowd because her face is the only one that isn't Japanese.

Karen-san, as she's known to her coworkers, works in Japan as a participant in an engineering-exchange program between Oregon-based Tektronix and NEC Toyama Ltd, a small subsidiary of the giant Japanese NEC Corporation. She and fellow Tektronix engineer Hiroaki Hayashigatani, an American of Japanese descent, are now wrapping up a six-month assignment that has taken them from one side of the Pacific to the other. Their assignment began with two months of intensive language study, followed by four months of engineering work.

NEC Toyama is located in the town of Nyuzen in the prefecture of Toyama. A coastal town of about 30,000 people located some 200 miles across the island of Honshu from Tokyo, Nyuzen is nestled between the Sea of Japan on its northern edge and the Japanese Alps to the south. NEC Toyama is

American engineer Karen Keough, on assignment in Japan, discusses a circuit-board flaw with a colleague.

primarily a producer of pc boards, as is the Tektronix plant at Forest Grove, Oregon, where the two American engineers will soon resume working. The exchange program was initiated in 1985 by Gene Hendrickson, manager of the Forest Grove facility, and Dr Shinichi Koyanagi, president of NEC Toyama.

Although the Americans' work

This article is the second in a series about engineering in Asia. It's the first of two articles about American engineers living and working in Japan.

duties at NEC differ little from their usual responsibilities at Tektronix, work conditions are another matter. Like most engineers in Japan, Keough and Hayashigatani work six days a week, usually from eight in the morning until ten at night. They wear uniforms. They get up from their desks twice a day and exercise to piped-in music. And at least once a week, on average, they go out with their colleagues for an evening of drinking. Keough is the only woman in the group; two women engineers from Tektronix completed exchange assignments earlier. Female Japanese engineers are rare.

The two Americans begin their workday by changing their shoes and putting on their NEC-supplied uniform shirts. There's an NEC logo on each shirt, and each worker wears a name badge and a button that bears the day's safety slogan.

The office where the two exchangers work is like most engineering offices in Japan, with rows of desks in a large open space. The arrangement of desks is hierarchical: supervisors look out over their engineers; the *kacho*, or section manager, watches the engineers as well as the supervisors; the *bucho* (engineering manager) watches all the engineers, the supervisors, and the *kacho*. Everyone can tell, simply by looking, his or her place in the pecking order.

Still, says Mary Mollison, a Tektronix engineer who worked in Japan in 1987, the structure is not as daunting as it may sound. "You *know* what your place is," she says, "and in some cases that's really nice, because there's no question, no ambiguity."

But if there's no question about your place, there's also no questioning of authority. When a *kacho* has

Kunihiko Suzuki, engineering manager at NEC Toyama, gives a word of advice to American engineers Karen Keough and Hiroaki Hayashigatani.

Most engineers in Japan usually work 14 hours a day, six days a week.

criticism for a junior engineer, explains Sue Galatz, a Tektronix exchanger who previously worked in Japan, the discussion is completely one-sided. The *kacho* calls the engineer up to his desk, and the engineer stands there, hands behind his back, looking down at the floor, while the *kacho* berates him, often shaking a finger in his face. It is unthinkable for an engineer to attempt a rebuttal, even when he's not at fault.

In one instance observed by Galatz and fellow engineer Ross McLaughlin, a Japanese coworker remained at work all night to repair some malfunctioning equipment and then, not having had time to go home for a clean shirt, was berated in the morning by his supervisor for being dirty. The weary engineer was shaking, says Galatz. "They really know how to intimidate," adds McLaughlin. What's more, the supervisor who did the intimidating had to endure a tongue-lashing himself from his manager. He is responsible for everyone in his group, and one of his group had failed to measure up.

Needless to say, such behavior cultivates fear. Mollison recalls walking down the hall one day with an engineer coworker when the *bucho* stopped them to ask a question. Mollison, like most Americans would, faced the *bucho* and made direct eye contact, but her coworker—under most circumstances "almost as confident as an American"—dropped his gaze to the floor and "broke out in a sweat, bigger than life." Before the short meeting was over, Mollison says, the engineer was mopping sweat from his face with his handkerchief.

But despite the rigorous environment, there's a certain camaraderie in the NEC Toyama engineering department, a kind of *esprit de corps* not unlike that of an army unit with a tough, but fair, sergeant. In fact, since Japanese engineers get promoted almost entirely according to seniority for the first 10 or 15 years of their careers, all those within a certain age group—not unlike a group of privates or corporals—are treated virtually identically.

NEC Toyama's tough but fair "sergeant" is Kunihiko Suzuki, the 43-year-old *bucho*. Military-trim, Suzuki has a no-nonsense attitude but projects personal warmth after hours. And it is after hours, in the ritual drinking sessions with colleagues, that Japanese engineers get a chance to vent some steam.

"It's a time when you can talk frankly with your boss over a couple of drinks," says McLaughlin, "and then the next day you can just go into work and say, 'Oh, I may have said some bad things last night. I drank too much,' " Galatz concurs.

"It's a given in their society that if you drink you can say whatever you want."

And they drink a lot, according to McLaughlin, because heavy drinking doesn't have the stigma in Japan that it does elsewhere. Furthermore, he says, you have to go along with the drinking or else miss out on the social interaction that exists in the after-hours sessions but is missing in the confined and very proper work environment. As Galatz discovered, joking around on the job is frowned upon. Having received a humorous fax from a Tektronix colleague, she laughed out loud as she read it at her desk until she glanced up and noticed everyone staring at her. Then she realized: "Oh, I'm not supposed to laugh. I'm at work."

But the drinking sessions serve as more than just a safety valve; they're also part of the famed Japanese process of consensus decision making. In the relaxed, free-wheeling atmosphere, engineers and managers alike become aware of their colleagues' *honne*, or true feelings, about different work-related issues. Sometimes problems get hashed out and decisions actually made over drinks; at other times, the sessions are merely a starting point for seeking agreement. In either case, the desire for harmony—a firmly entrenched and highly characteristic feature of Japanese society—underlies even the raucous celebration of a night on the town.

Suzuki explains, however, that while the result of consensus building is harmony, the process of reaching a consensus is often much less harmonious. There are plenty of "hot" meetings, he says, that precede the official meetings in which decisions are formalized.

"There's a lot of hashing back and

Tektronix engineer Hiroaki Hayashigatani is a Nisei, an American whose parents were born in Japan. Although he was already fluent in everyday Japanese, he had to acquire a new technical vocabulary for his work at NEC.

forth," agrees McLaughlin, and there is a lot of input to decisions. "They're not made in a vacuum," he notes. McLaughlin continues: "A decision, say, that involves a certain manufacturing area will have representation from management, engineers, and people that work on the equipment daily, to maintenance technicians—all levels."

But, say McLaughlin and other Tektronix engineers, the hierarchical structure of Japanese companies also comes into play in decision making; decisions are not entirely the result of consensus, because they do go up the chain of command for approval, and sometimes they actually emanate from somewhere up the chain. Hidebumi Ohnuki, an NEC engineering manager who worked at Tektronix as an exchanger in 1986, concurs: "We have two styles of management, top-down and bottom-up." But however a decision is made, he says, "it's always very clear which way we should go."

It's not always clear after a meeting of Americans, though, say Ohnuki and Yutaka Makino, an NEC engineer who completed an exchange assignment at Tektronix a year ago. "They have so many opinions," Ohnuki says, "and sometimes they cannot decide which way is best." For Makino, the American meetings were so overwhelming, with all the participants engaged in simultaneous, rapid-fire talking, that he could only sit back and watch in bemused wonderment. Engineering manager Suzuki actually thought the first meeting he attended in the United States, 18 years ago, might result in a fight; he marveled when the participants left their disputes behind them and walked away in good spirits.

Compared with American meetings, the Tektronix engineers found NEC meetings formal and tame. No one ever brings food or drink to a meeting; at daily briefings, participants don't even sit. The meetings are much more focused, and attendees are much more willing than Americans to be followers rather than leaders.

Indeed, there is a strong, overall cultural pressure in Japan not only to be a good follower but—even more significant—to avoid any behavior that attracts attention. There's a frequently quoted saying: The nail that sticks up gets hammered down.

For engineers, there's little incentive to get attention anyway, since promotions for younger engineers are based solely on seniority. "You know when you come here," says Keough, "that you're going to be a freshman engineer for so long, and then you're going to move into more responsibility, whereas in America I might think as soon as I [begin a job] that if I do something fantastic I'm going to move right up." There's very little reason for a Japanese engineer to even compile a resume. Job changes are rare; most engineers spend their entire professional lives at one company.

But Hayashigatani notes that Japanese engineers get rewarded for being good followers, so they don't really need to be leaders. The result, he says, is that you can gauge a person's level of seniority even by his actions. "They tend to have more humility if they're lower," he comments. "It's evident from the respect they show their elders."

Japanese engineers returning from an extended assignment in America are not so humble, apparently. They're "aggressive," says *bucho* Suzuki, to which Keough responds with "assertive" as a possibly more accurate description. "Ag-

If there's no question about your place in the hierarchy, there's also no questioning of authority.

gressive!" insists Suzuki, and they laugh.

"They're tigers," agrees Mollison, who observed some returning Japanese engineers during her NEC assignment. The difference between those who have worked abroad and those who haven't is remarkable, she says. Mollison wonders, though, whether the newly confident travelers will eventually get hammered down like the proverbial nail. Engineering manager Suzuki, however, claims to have no problem with aggressive attitudes as long as everyone goes along with decisions once they're made. And do the returning Japanese engineers go along? "Of course," he insists. "Yes, they do."

But whatever problems may arise on a return from abroad, an assignment in the United States is still a feather in an engineer's cap, according to Mollison. With promotions based mainly on seniority, a foreign assignment might not be accompanied by an official rise in status, but it's nevertheless indicative of an engineer's presence on the fast track.

The engineer probably has no say about his assignment, however, either in requesting it or in deciding whether or not to accept it. Management decides who will be transferred, within or without Japan, and the selected engineer merely complies. Furthermore, when Japanese engineers get transferred, their families seldom move with them. Prolonged separations, some lasting several years, are common. Suzuki, for example, has lived alone in Nyuzen for the past four years; he visits his wife and children, who live near Tokyo, about once a month.

As the Tektronix engineers observed, Japanese engineers' lives differ from Americans' in other ways, too. A central difference is that the Japanese are much more likely to be technical generalists, a fact which has ramifications throughout their careers. They begin with a broad engineering education that offers much less of an opportunity to specialize than American curricula do; their general education continues after graduation at the company where they choose to work.

Over a period of several years, new engineers complete a variety of assignments in various technical areas. Company managers determine the assignments of individual engineers and, ultimately, what each engineer's specialty will be. This approach offers the advantage, most Japanese engineers believe, of providing broad experience that's helpful—and, to the Japanese way of thinking, almost indispensable—when an engineer moves into management.

In keeping with the concept of strong management, design engineers are closely supervised. Managers continually look over designers' shoulders, says McLaughlin, but they are always well qualified to do so, having come up through the technical ranks themselves. Further, the close supervision merely accompanies the process of consensus decision making; it does not reflect lack of trust in the designers. "There's a lot of room for individual creativity. You're not given free rein, but you are given a long leash," McLaughlin says. And, says Mollison, "If you look at [the equipment they design], you would say they're being *very* creative."

Mollison performed some creative work herself during her NEC assignment. Engineering manager Suzuki recalls her being "very clever—almost too smart for me!" But even though Mollison feels her Japanese coworkers bent over backwards to accept her not as a woman engineer, but simply as an engineer, she says there were gender barriers to overcome nevertheless. Whether in Japan or the United States, she asserts, women engineers often have to disprove the tacit assumption that because they're female they're not technically astute.

Cultural differences, rather than outward discrimination, were what Galatz grappled with during her stint at NEC. Japanese men simply don't know how to talk with women, Galatz maintains, especially women of equal professional stature, a rarity in Japan. Galatz often felt excluded from conversations; if she attempted to start one

It is after hours, in ritual drinking sessions with colleagues, that Japanese engineers get a chance to vent some steam.

Exchange engineer Sue Galatz shares after-hours drinks and fun with NEC coworkers. (Photo courtesy Sue Galatz)

herself, she frequently got only one-word replies. But, she notes, "I didn't ever feel that somebody didn't want to work with me because I was a woman." And, Galatz adds, "In America, I've been discriminated against as a woman in the workplace much more than I was over in Japan. I've had summer jobs where people would say really rude things, which *never* happens in Japan."

The Japanese electronics industry's long workdays, of course, are completely nondiscriminatory—all engineers and managers have them. At NEC Toyama, Galatz says, "There's a huge social pressure. If the person sitting next to you is staying and working late, you better be there, too. If the boss is working late that night, and he sees that that person is there and you're not, formally there's no mark against you, but informally there is."

In order to make it through their 14-hour days, Japanese engineers pace themselves, Tektronix exchangers say, and the result is inefficiency. "We are much more efficient during the time we're at work than they are over there," comments Mollison. McLaughlin adds that Japanese engineers he worked with often mentioned feeling burned out from the constant pressure of deadlines and long hours, and that they candidly admitted making "dumb" mistakes and not working creatively.

The burn-out problem hasn't gone unnoticed, however. "The *bucho* of engineering talked to us," Galatz explains, "and said, 'Look, we realize in Japan people work very hard and they work long hours, and we are trying to control that.' " So the first Wednesday of every month, continues Galatz, "they have the you-must-go-home day—no overtime. At 4:45, this woman comes on over the speaker and says, 'It's no-overtime day; you have to go home at 5:15.' "

Japanese engineers do get paid for overtime work, though. They also get substantial bonuses. Mollison and Galatz, who as Tektronix employees remained on its payroll during their stints at NEC, exchanged pay information with Japanese colleagues and found that their compensation was virtually the same after overtime pay and bonuses were added and taxes were deducted. And although it hasn't yet had a major impact, there is a growing trend in Japan to shorten workdays and to adopt a five-day work week. As the country's export markets mature or face possible restrictions by foreign governments, there is increasing incentive to give citizens more leisure time for spending money and stimulating Japan's domestic economy.

For Americans working in Japan, the long work days and highly structured work environment are the two greatest barriers to job sat-

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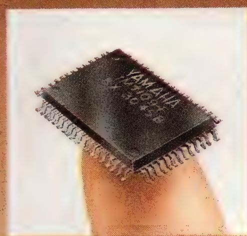

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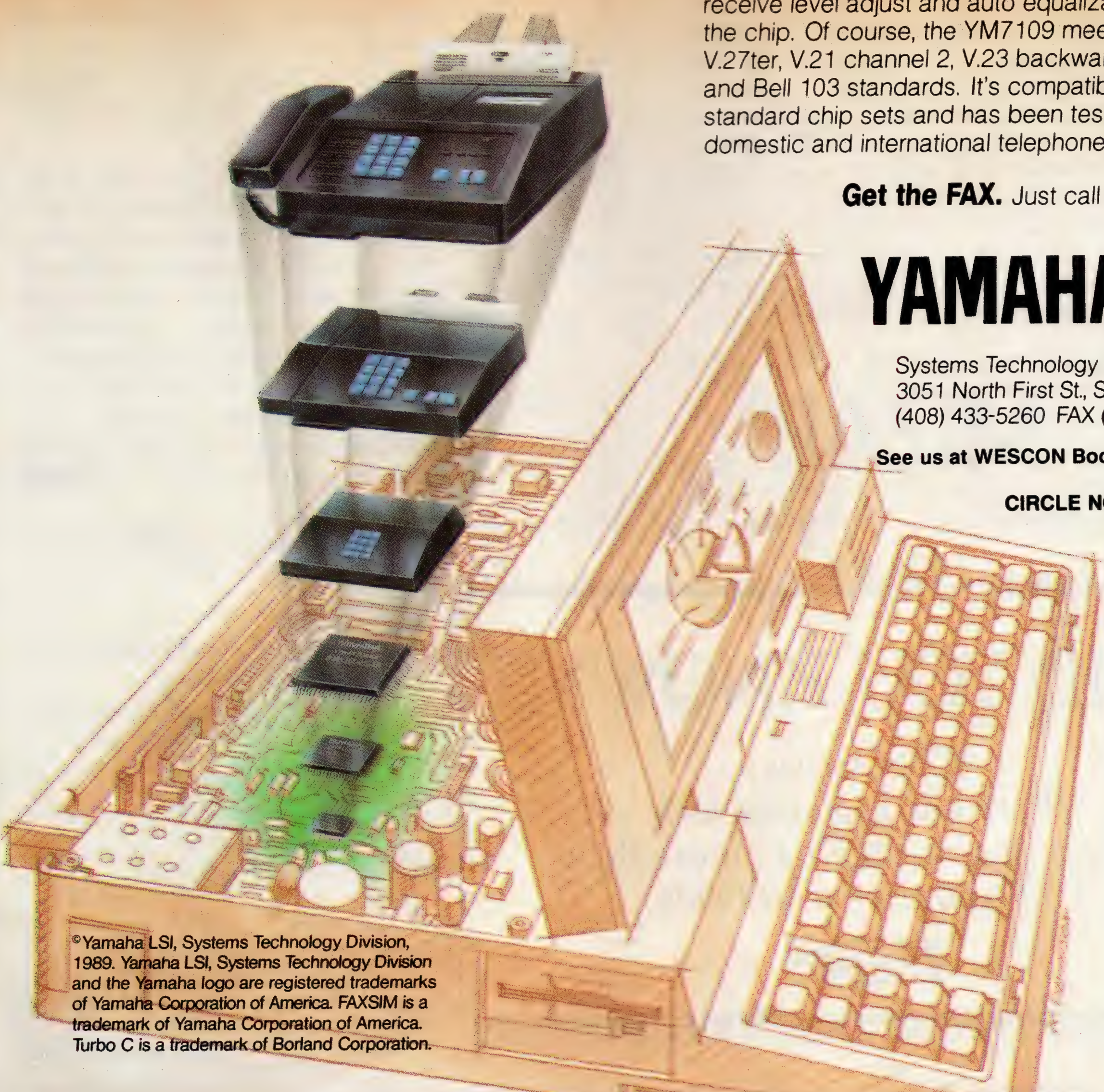

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isfaction. Outside the office, there is the additional stress of adjusting to cultural attitudes that are probably as different from American customs as any in the industrialized world. Some Japanese even exhibit blatant discrimination toward *gaijin* (foreigners), a not unexpected result in a society as racially and culturally homogeneous as Japan's.

But Tektronix exchange engineers say discrimination is not a constant problem, and cultural difficulties are largely a result of unfamiliarity; Japanese who have had extensive contact with Americans tend to be friendlier and much more communicative. In general, the exchangers say, Japanese are very warm, although they may be reserved in displaying that warmth until they get to know someone well.

Mostly, say the Tektronix engineers, working in Japan provides an opportunity to gain new perspectives. Indeed, the main objective of the exchange program, according to Mollison, is to "grow people into global thinkers, to make them more far reaching in the way they look at things." Without exception, the exchangers agree that the program achieves that objective. **EDN**

In the next issue of EDN: Life in Japan outside the office.

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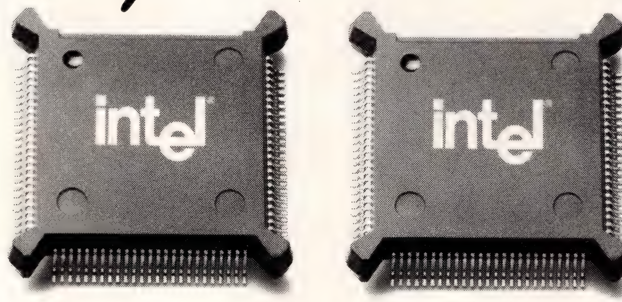

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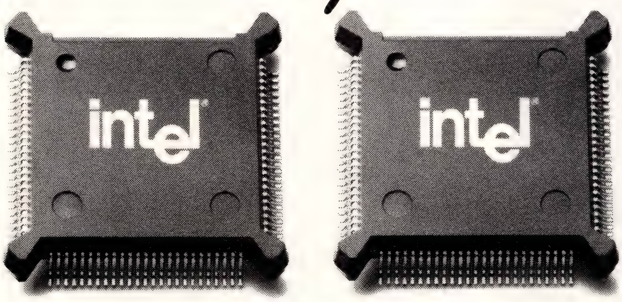

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IN-CIRCUIT EMULATION

ICs and tools tame tough technology

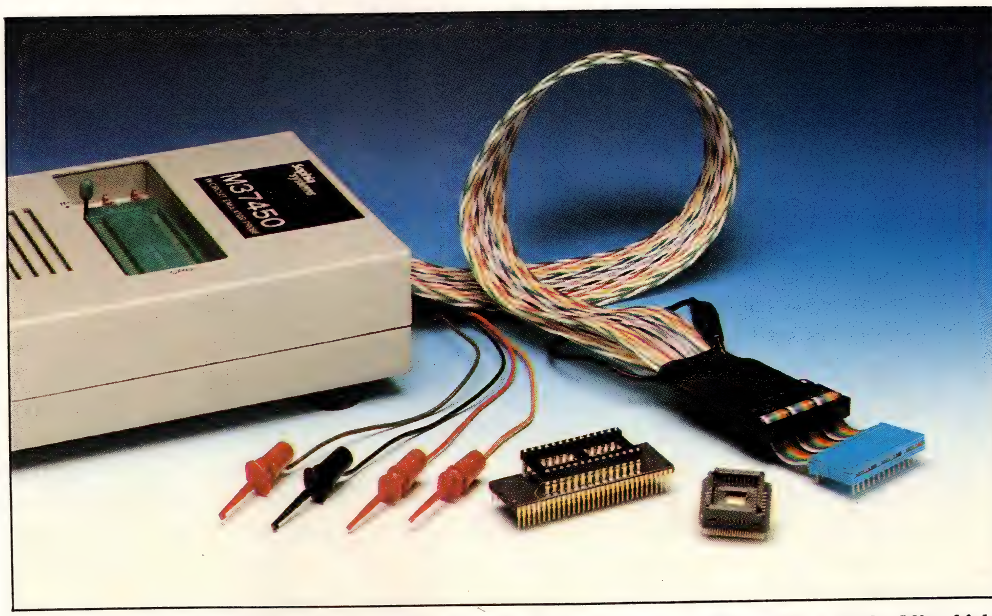
High-performance μPs were poised to kill ICE, but new design techniques for both the chips and the instruments have given this vital debugging technique a new lease on life.

Dan Strassberg, Associate Editor

The word was out: In-circuit emulation (ICE) was dying. Unable to withstand repeated assaults from increasingly powerful processors, ICE, the faithful friend of embedded-system designers, had taken to its bed to await the "ice man." Clock rates of 25 MHz and above, pipelined instructions, on-chip caches and cache controllers, buses with one cycle per processor-clock cycle, and a host of other innovations in μP architectures had proven to be too much for ICE. New types of intelligent chips—RISC, DSP, and video processors—simply compounded the problems. Even μCs, which tend to treat information crucial to ICE as something to which no outsider should be privy, were delivering body blows.

But a funny thing happened on the way to the funeral—chip vendors realized that many system designers, especially those working on real-time, embedded applications, just couldn't debug time-critical code effectively without the help of ICE. If those designers felt that problems in applying emulation tools to the marvelously powerful new μPs were likely to slow down system debugging, they would, wherever possible, stick with older, lower performance processors. The result would be unsold ICs and red ink. So chip designers went back to the drawing board and incorporated features in their silicon to facilitate emulation.

Meanwhile, emulator designers, a hardy breed accustomed to working on the frontiers of technology, attacked the



*A **device-packaging innovation** is one way Sophia Systems improves the visibility of the Mitsubishi M37450 μC's internal nodes. The emulation processor is in a special 40-pin DIP topped by a 28-pin socket. For code development before you have a target system, plug the probe into the emulation processor's socket and plug the μC into the ZIF socket in the pod.*

problem. Innovations in circuit design and packaging have yielded a significant number of emulators that extend the capabilities of in-circuit emulation. In many cases, these products depend on features included in µP chips to aid in testing and debugging. But regardless of the technology emulators use to achieve higher performance, system designers can count on ICE's help in debugging products based on most of the high-performance processors available today as well as those likely to be available for several years to come.

Indeed, in the words of Dick Odom, vice president of engineer-

System designers can do much to ease use of ICE

In researching this article, EDN asked several ICE vendors what their customers—system designers—should do in their designs to make debugging with an ICE as painless as possible. The design staff of Applied Microsystems contributed a particularly extensive and well-thought-out answer that became the basis for the following tips.

Care in hardware design fends off debugging woes

In the hardware area, observe these precautions:

- Don't push the specs. Keep the clock-to-processor-pin timing as loose as possible. In emulators, the signals with the longest delays are clocks. Use a robust clock driver to reduce the effects of emulator loading.
- Understand that emulators, like scopes and logic analyzers, add a little capacitive loading to the signals they monitor. Be prepared to add pull-up resistors when the fan-out is high.
- Use the nonmaskable-interrupt function sparingly. Many emulators use this function to interrupt program flow. If you use this interrupt for other purposes, conflicts can result. To avoid such conflicts, you can latch the interrupts your system generates and OR them with the emulator's nonmaskable interrupt.
- If you use a socket for the CPU, make sure the target system can accommodate the emulator probe. Orient the CPU socket so that the routing of the cable doesn't excessively constrain the pod location. **Ref 1** covers this subject in detail.
- Don't mix CMOS and TTL. If you do, expect to have initialization problems each time you apply power.

In the software area, be aware that one of the most important "consumers" of embedded source code is the person who will be integrating the product's hardware and software using an emulator and source-level debugger. Timely and accurate emulation and debugging depend on clear and complete information, a requirement that increases in importance as the code becomes more complex. Even if you are the one who debugs the code you write, you will *save* time by devoting a little *extra* time to clearly documenting your work.

Provide adequate resolution in your high-level code. One complex line may provide the function you need, but when you use an emulator or debugger to single-step through the code, the steps will be so large that they bypass crucial information. The following C code is too compact:

```
If ((allocate(len(msg) + 13)) = = check (arg))
  {. . .
```

The line combines several data-gathering procedures with a decision-making instruction and buries the results of some operations. Single-stepping through this C code won't reveal why the branch worked or didn't work. To find out, you'll have to use an assembly-language debugger to single-step through the equivalent machine-language code. In so doing, you lose the speed and accuracy of programming in a high-level language.

A better approach is to write code that lets you see an appropriate amount of detail at each step.

```
entry_length = len(msg);
record_size = allocate(entry_length + 13);
record_ver = check(arg);
If(record_size = = record_ver)
  {. . .
```

This code is easier to comprehend and maintain. Each line performs a manageable amount of work, letting you observe appropriate detail at each step. Debugging at the source level will reveal why the branch succeeded or failed.

Make data visible. When you expand code, as above, you also make your data more visible. You will want to monitor the data as you work. If you provide a hook in the form of a variable, the data will be easier to use during emulation.

ing at emulator vendor Microcosm, "Doom sayers have been predicting the demise of ICE almost from the time it was invented. Yet, today ICE isn't merely alive, it's thriving, and we have confidence in our ability to keep it thriving for the foreseeable future—regardless of the innovations chip designers create."

Nevertheless, ICE faces competition from several debugging techniques, each especially suited to a particular part of the hardware and software development process. Dick Jenssen, vice president of product development at Applied Microsystems, a leading supplier of high-performance emulation tools,

```
entry=table(index);
display(entry);
```

The code above will make the results of the table procedure visible in a variable named "entry," which you can monitor while you work. The same function in a more compact style will bury the result of the table procedure:

```
display(table(index));
```

Write descriptive code. A lot has been written about making code more usable by making it more descriptive. Designing code for use with emulation is a case in which you get real benefits in accuracy and productivity. The code is the primary source of information for a person using an emulator. The more complete and understandable the information is, the more effective debugging will be. Cryptic names provide minimal information.

```
If(x= =cd && m!=bks{
  n- -;}
else    {
   n=rp(cp);}
```

This code is difficult to work with, with any degree of speed or accuracy. You must constantly guess about the nature and function of the data and procedures. Mistakes are virtually inevitable. The equivalent code, enhanced with descriptive symbols and comments, promotes quick, accurate integration.

```
If(input= =char_delete &&
              code!=backspace){
        position- -;}
else    {
        position =reposition(char_place);
/* valid range for char_place: 0 - 79 */
```

Partition code to keep time-critical sections separate from the rest of the program. Doing so makes tracking critical sections easier.

The selection of the correct tools is at least as important as using the tools intelligently. Here are some suggestions about when and how to select tools:

- Plan to purchase an emulator early in the design cycle. That way, you'll know how to use it *before* you are under the gun to debug a critical problem.
- Select appropriate tools. Use a compiler designed for the creation of embedded code; not all compilers produce the comprehensive cross references debugging hardware requires. Don't use a simulator to debug time-sensitive problems.
- Schedule time for the integration of hardware and software. As a rule of thumb, when a programmer delivers code, you should expect about 50 bugs per 1000 lines. After rigorous testing, there will still be 5 bugs per 1000 lines. Integration takes time, and you should schedule this time.
- Accommodate tool characteristics. Most development tools have limitations. Perhaps the variable names your debugger can display are shorter than those permitted by your compiler. If you are using a tool that displays only the first 10 characters of a variable name, make sure that those characters are significant. For example, if you have elements called "name.operator.one" and "name.operator.two", they may both show up in a debugger window as "name.operat". Confusion and errors will be unavoidable. If you know the debugger's limitations before you use the compiler, you can select names you won't have to change.

classifies the problems encountered by system developers into three major categories: logical, run time, and real time.

Three classes of problems

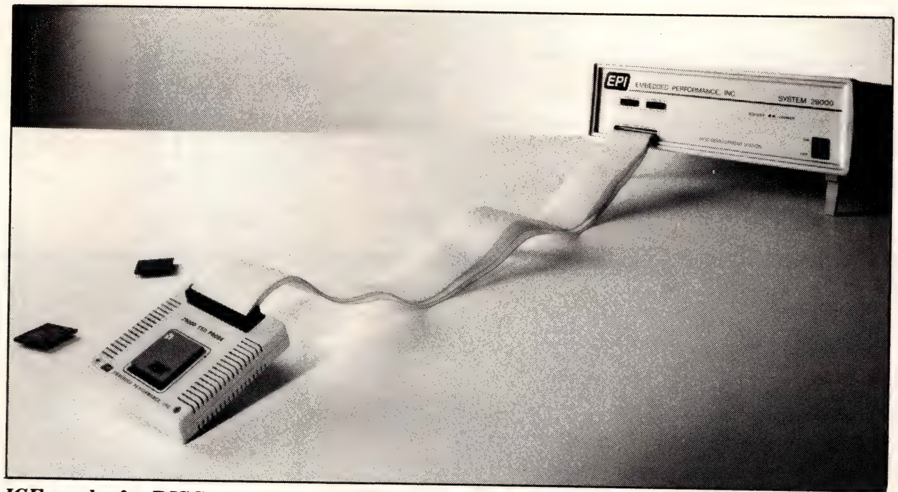
Logical problems are basic flaws in the program logic and are unrelated to hardware. If you program in a high-level language, a high-level-language debugger will catch them. CASE (computer-aided software engineering) tools are intended to prevent such problems.

Run-time problems are not time critical. They will occur even if you slow down program execution. Although you can use ICE to catch these problems, you can also find them with a machine-language debugger.

Real-time problems usually occur because of hardware/software interaction. Debugging them requires running the system at full speed, that is, in "real time." Ideally, you should not have to slow the clock or add wait states. Furthermore, in the terminology of ICE vendors, the debugging tools should be nonintrusive; that is, the debugging hardware should not affect normal system operation by, for example, usurping system resources such as I/O ports or nonmaskable interrupts.

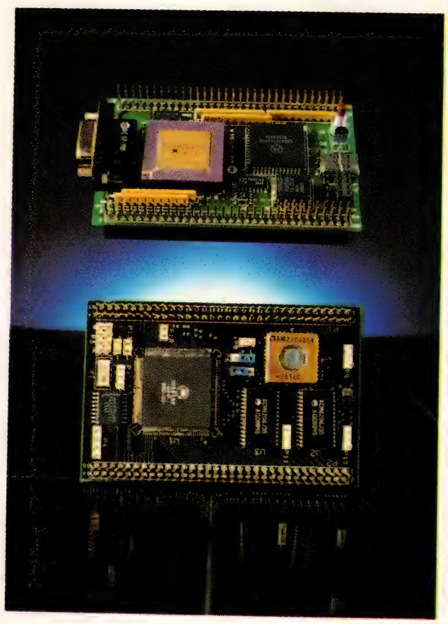
Beside ICE, tools that you can sometimes use to good effect on real-time problems include general-purpose logic analyzers. Some engineers maintain that if you're handy with a logic analyzer, you don't need an ICE. On the other hand, ICE vendors, while agreeing that a logic analyzer can be a powerful debugging aid and an adjunct to ICE, argue that a general-purpose logic analyzer is rarely a substitute for an ICE. Instrumentation leader Hewlett-Packard appears to hold the latter opinion; HP makes both ICEs and logic analyzers.

Implementing other emulation techniques—ROM emulation and bus emulation—is generally easier than implementing ICE. These techniques differ from each other and from ICE in how they access the target system. A ROM emulator plugs into a socket in which you'd normally plug a ROM; a bus emulator (sometimes called a card-edge emulator) connects to the system bus, usually at a card edge, and takes control of the bus for testing purposes. Neither technique provides as much visibility of the processor's operation as does ICE.



ICE works for RISC *processors, too. This system, from Embedded Performance Inc, is for AMD's AM29000 and is priced from $11,900 to $26,000.*

An in-circuit emulator connects to the target system at the microprocessor socket. In practically all cases, the ICE plugs into the µP socket in place of the processor. The ICE contains an emulation processor that substitutes for the target processor during emulation. Because the first commercial ICEs came from a chip vendor (Intel, a company that continues to manufacture development tools) and because chip vendors can create custom chips with relative ease, ICEs developed a tradition of using special versions of their target µPs as emulation processors. These proprietary "bond-out" chips have usually been standard dice in special packages with extra pins. The extra pins let you access internal nodes on the chip to provide visibility and control of the processor's operation.



Though not an ICE, *this evaluation unit for Motorola's 68332 32-bit µC facilitates application development. Included on the small board are a processor, 128k bytes of EPROM, 64k bytes of RAM, an RS-232C port, and a development interface that uses an 8-bit 68HC11 µC.*

ICEs without bond-out chips

In cases where the processor vendor supplies development tools, bond-out chips may be completely unavailable to third-party tool ven-

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dors. Even when processor vendors are not in the development tool business, if they produce bond-out chips at all, they do so in low volumes. Tool vendors find these chips both hard to obtain and expensive. Therefore, many ICE vendors avoid using bond-out chips, and the evidence suggests that they don't *have* to use such chips to design a competitive ICE. Indeed, there are many examples of ICEs—even ones for very complex processors—that don't use bond-out chips and yet insert fewer wait states than do emulators that use the specialized chips.

Furthermore, as processor complexity grows, IC vendors speak of the need to design bond-out chips that differ considerably from standard chips. An emulator for a high-performance µP can require visibility of so many circuit nodes that the bond-out chip requires a unique mask set. Interconnecting internal nodes to pads at the chip's periphery can even necessitate extra processing steps. Chips made in such special ways can exhibit significant differences in performance from standard parts. Because IC vendors produce bond-out chips in such small quantities, the chips are expensive to begin with; the more special processing they require, the more expensive the chips become.

Even worse, the greater the development effort required to produce a bond-out chip, the later in the life cycle of the µP it becomes available. Without some means of keeping the design of bond-out chips close to that of standard µPs, ICE vendors that rely on bond-out chips would have to significantly delay the availability of ICEs, and designers of embedded real-time systems would have to delay using new µPs until well into the chips' life cycle.

This problem is only one of the reasons Intel's chip architects work closely with the company's development-tool designers almost from the start of new µP projects. So far, the most visible results of this partnership are the breakpoint registers incorporated in Intel µPs, beginning with the 80286. The 80386 has four such registers; you can specify whether each one contains a data-access or a code-execution breakpoint. Circuits on the chip constantly monitor the µP's instruction and memory-address registers. Depending on what you specify, when the data or memory address matches a breakpoint, the monitoring circuits generate an interrupt.

In addition to breakpoint registers, the high-performance 32-bit processors in the 80960 family include a trace-control register, which provides seven modes of trace control that you can use individually or in combination.

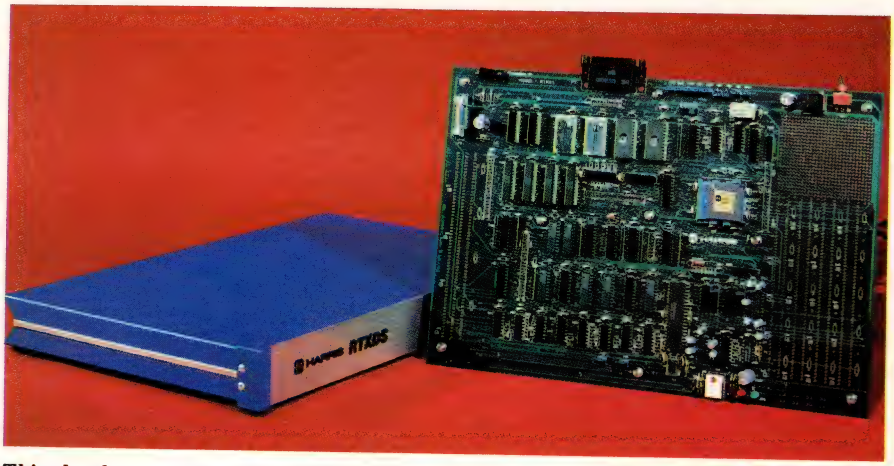
Intel is far from the only vendor to bring chip architects and tool designers together early in a µP's development, although it is probably the company best known for doing so. Even smaller companies like Analog Devices, whose µP offerings are limited to DSP chips and which has no development-tool operation of its own, work closely with ICE vendors early on. Analog entered such partnerships during the development of its ADSP 2100 and 2101 16-bit DSP processors.

ICE isn't for everyone

Not every developer of µP-based systems depends on ICE, however. Designers of personal computers and workstations generally introduce products based on new µPs very early in the processors' life cycle. As a consequence, these designers have had to evolve work styles that depend on tools they can get shortly after a processor's introduction. Fortunately, computers and workstations generally don't exhibit the time-critical hardware/software interactions that are so important in embedded real-time applications.

Some µPs show strong evidence that their designers intended them for use in workstations. For example, features that could ease emulation are absent from RISC chips from Sun Microsystems' SPARC series and those from MIPS Computer Systems. Neither Sun nor MIPS sells these chips on the open market, but they have licensed other companies to do so. LSI Logic is one company that sells chips from both families.

Don't get the impression, however, that because a processor is a



This development board, *available cased and uncased, works with Harris Corp's RTX 2000 µCs. You program these processors in Forth; the vendor claims that Forth encourages the development and debugging of code at a module level that obviates an ICE.*

In-circuit emulation

RISC chip, it *can't* be designed with emulation in mind. Advanced Micro Devices' AM29000 is a RISC processor designed for embedded applications. AMD began working with vendors of hardware and software development tools early in the chip's design cycle. Among the AM29000's emulation-support features is a halt mode. The feature adds only three pins to the device. Aware of the importance of development tools to embedded-system developers, AMD has announced a program called Fusion 29k; the IC vendor publishes a list of tool suppliers that have announced or are planning support for the AM29000. One highly prestigious vendor on this list is Hewlett-Packard.

Texas Instruments has made some of the most sweeping and impressive-sounding changes in the way µPs work with emulators. The TMS320 series of DSP chips will enter its fifth generation when TI begins sampling the TMS320C50 early in 1990. Like several of its predecessors, the C50 incorporates a serial port through which you can obtain a great deal of information about the machine's internal states. Unlike earlier chips, the C50's serial test port conforms to the JTAG (Joint Testability Action Group) standard, also known as IEEE P1149.1. In fact, the port supports a *superset* of P1149.1.

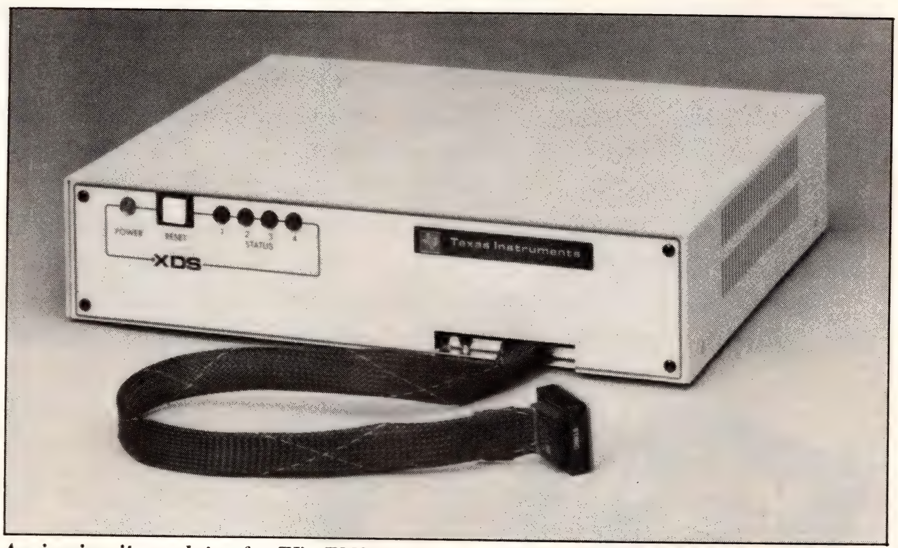
During operation of the processor, you can capture a "snapshot" of the chip's test nodes in special internal registers. Taking this snapshot scarcely slows the chip's operation. Then, while the processor continues to operate at full speed, you can shift the register's contents out through the testability port one bit at a time. This process provides a view of the processor's state, albeit a slightly retrospective one. According to TI, the cost in chip area of this JTAG port is surprisingly small. The company's engineers have found a way to place most of the extra supporting circuitry near the periphery of the chip in areas also used for power busing. Furthermore, TI says the scheme lets you perform the functions of an in-circuit emulator by using a small IBM PC bus-resident card in combination with a general-purpose logic analyzer.

Despite their complexity, *Intel could introduce an ICE for the 80960 series of µPs a few months after announcing the processor family due to cooperation between the company's chip and tool designers.*

TI claims that this scheme is one of those rare situations in electronics where everybody wins and nobody loses. Among those who benefit from the JTAG port are designers of embedded systems who use the port for debugging their code; TI's own test engineers, who use the port for testing devices prior to shipment; customers' test engineers, who use the port for testing the chips once they have been loaded onto boards; and customers' field service engineers, who can use relatively inexpensive equipment to test processors in the field.

According to TI, the JTAG port may even be instrumental in breaking down the legendary barriers that exist between design, production test, and field service in most companies. "You won't have designers cursing production test people who ask for more test points, and both groups acting totally unsympathetic to field service's requests for "hooks" for attaching low-cost testers in the field," says Gary Swoboda, senior member of the TI technical staff for the 320 family. "For once, everyone can support the same test and debug mechanism."

But good as it may sound, the JTAG port isn't for everyone. TI's



An in-circuit emulator *for TI's TMS370 family of 8-bit µCs uses two standard chips as one emulation processor for standard and custom µCs, which the vendor will produce in quantities of 50,000 or more. This technique makes emulation available early in the target-system development. The TMS370 XDS/11 ICE costs $2850.*

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In-circuit emulation

TMS370 series of 8-bit microcontrollers uses a different scheme, and Swoboda concurs that the 370's approach is more appropriate on these less complex parts. For one thing, on smaller chips, the JTAG support circuits would increase chip area by an amount you'd have to call significant.

The 370 series is a family of μCs, most of which include resources, such as ports, timers, and ADCs, that tailor them for specific applications. Many members of the family can't access significant amounts of memory off the chip. TI has minimized the problem of creating bond-out chips for the series by making the functional equivalent of bond-out devices from pairs of ICs. One member of the pair is a general-purpose CPU; the other incorporates the I/O functions of the emulated part. Between them, the two chips have more pins than any single 370 device. The extra pins perform two functions: They enable the two devices to communicate with each other so that they can function at full speed as a single device.

For more information . . .

For more information on processors and development tools such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know that you read about them in EDN.

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In-circuit emulation

They also provide the internal-node visibility required for emulation.

This brief survey of techniques used by chip designers to facilitate emulation provides only a partial view of the activity in the field. Bercause the requirements for the visibility of a µP's internal nodes for testing are not too different from the requirements for their visibility during emulation, you can expect to see a degree of synergy—advances in µP testability will help emulator designers create products that keep pace with advances in µP performance. The testability revolution has set some of the most creative minds in the semiconductor industry to work in an area where some of the most creative minds in instrumentation were already at work. The combination is so potent that accurately predicting what wonders will unfold is nearly impossible. EDN

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2. Leibson, Steven H, "In-circuit emulators for µCs probe software activity in a closed environment," *EDN*, July 20, 1989, pg 64.

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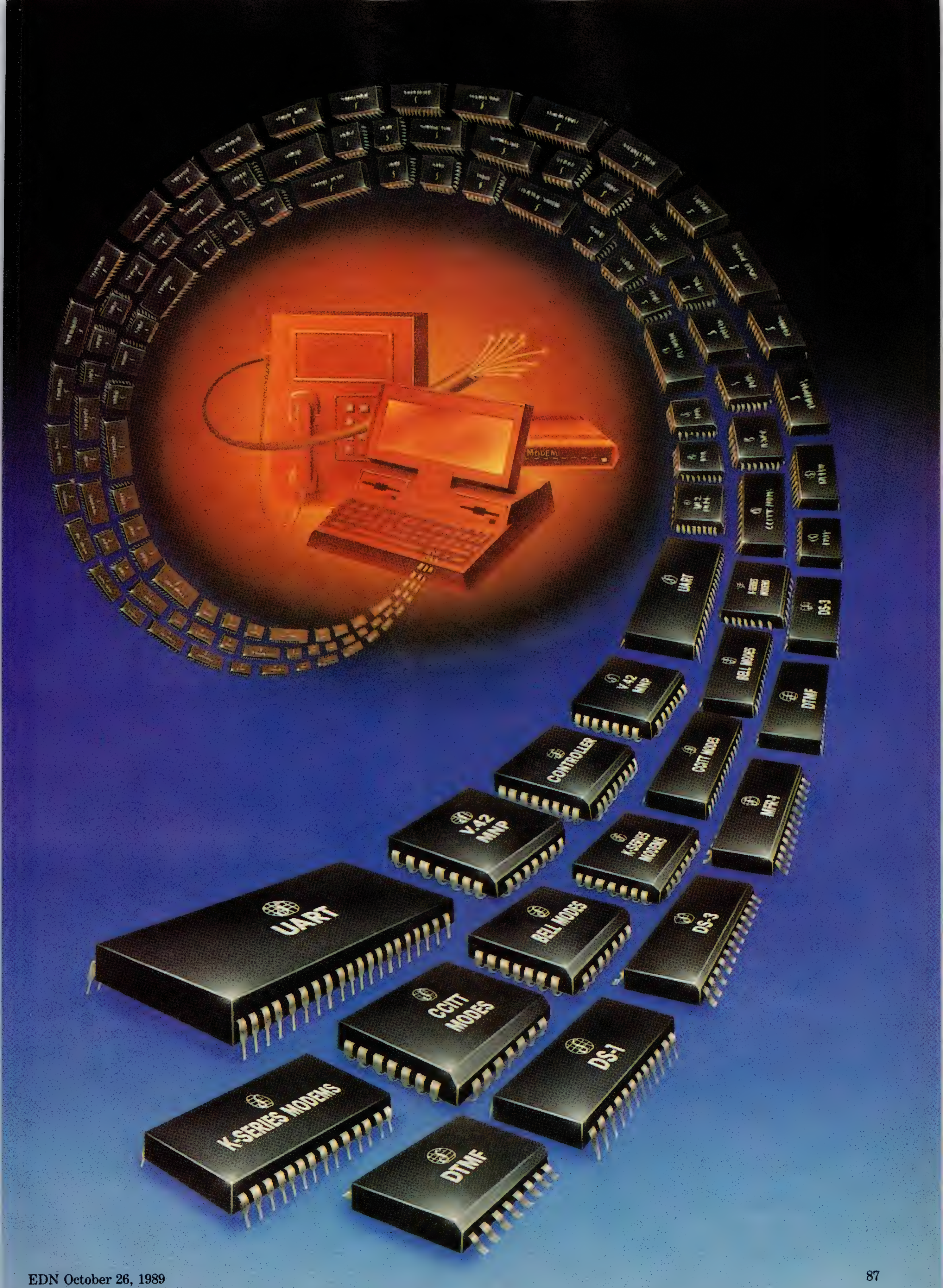
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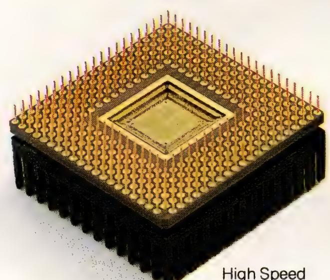

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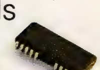

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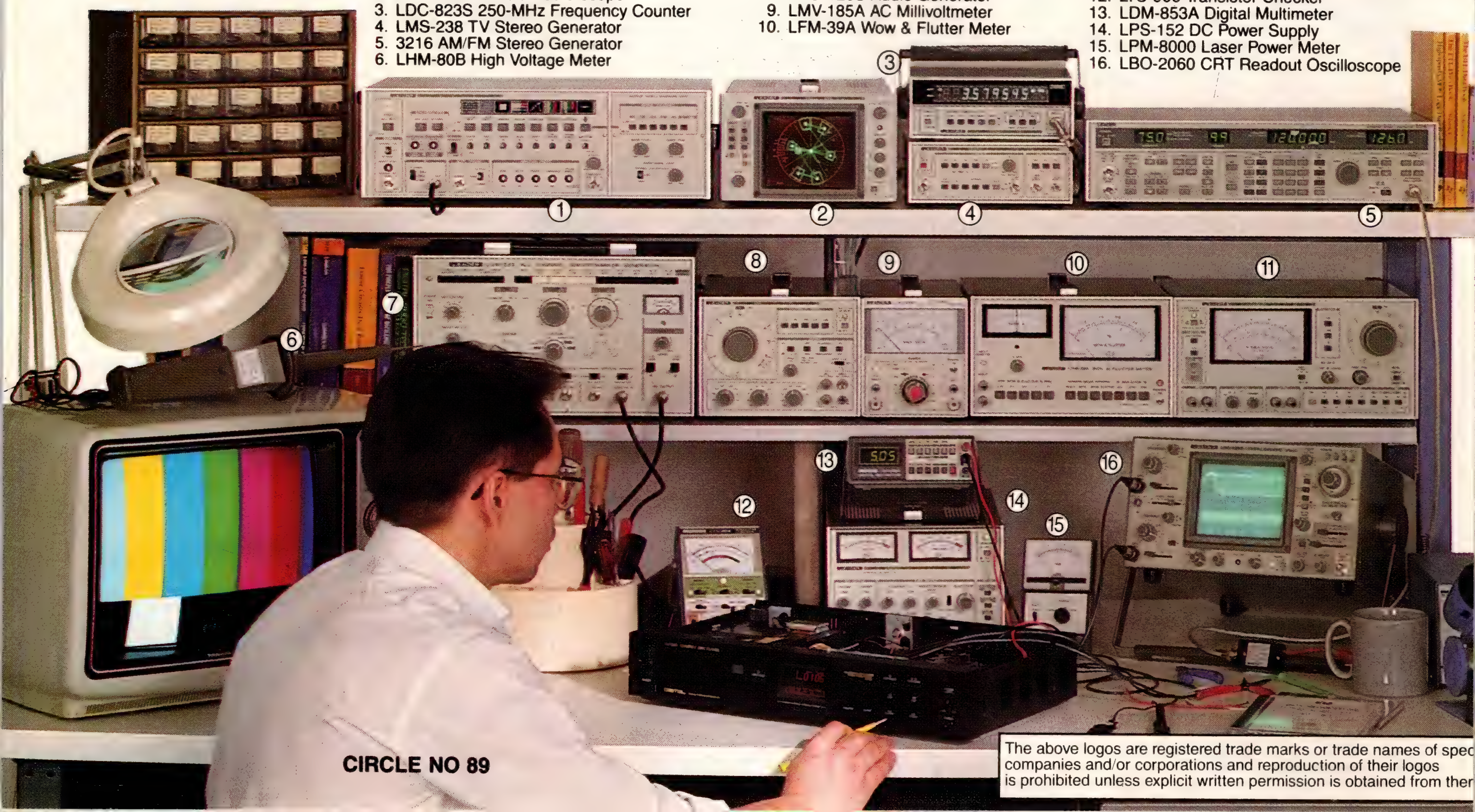

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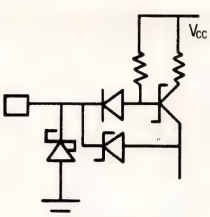

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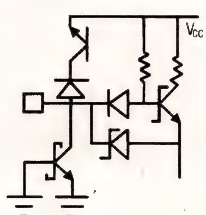

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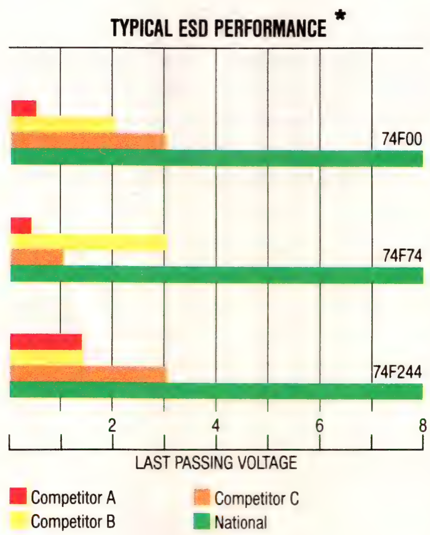

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DMA CONTROLLERS

Adding DMA to other functions boosts speed

You get improved performance, reduced cost, and a simplified design when IC designers integrate DMA controllers with other devices.

Steven H Leibson, Senior Regional Editor

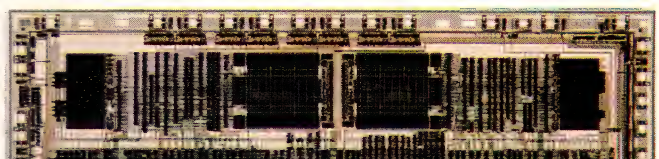
You can't beat DMA for high-speed data transfers in a µP- or µC-based system. DMA controllers (DMACs) waste no bus cycles to fetch instructions; these hard-wired machines already know how to do the job. DMACs are really zero-instruction-set computers and offer superior performance to even the much-publicized reduced-instruction-set computers (RISCs), at least for transferring data.

Because they provide the highest possible data-transfer rates, DMACs quickly became an essential component in the µP's support-chip retinue. Today, however, DMACs appear to have been almost totally eclipsed by the 32-bit processor architectures introduced by semiconductor manufacturers during the last two or three years. In fact, many IC vendors currently offer no DMACs or 16-bit controllers to support their highly touted, 32-bit RISC and complex-instruction-set computer powerhouses.

But the DMAC isn't dead yet. It has simply moved into other types of ICs and fused with other IC functions. These hybrid controllers can deliver performance superior to a multichip solution in a form that's easier for you to use in a system.

One company, Siemens Components Inc, continues to advance the idea of discrete DMAC ICs. Siemens developed its 4-channel 82257 DMAC a few years ago, and it's still available for $30 (1000). However, Siemens has upgraded the 82257 design twice, and the latest product of that evolution is the 82258A advanced DMA (ADMA) IC.

The 82258A supports only 8- and 16-bit flow-through transfers, (see **box,** "DMA basics: flow-through and fly-by transfers"). Rather than build a 32-bit device, the 82258A's designers chose to use additional transistors so they could include other capabilities. For instance, one of the 82258A's four DMA channels supports a multiplexed mode that services as many as 32 devices without µP intervention. The 82258A also sports features such as data comparison and matching (which terminates a transfer or triggers a change in transfer parameters when a match occurs), verification



***Many high-speed peripheral devices,** such as this Z16C30 universal serial controller from Zilog Inc, provide DMA control on the chip to support the IC's high data rates.*

(which compares two data blocks without moving data), and translation (which uses a translation table to perform data conversion on the fly during transfers). A 10-MHz 82258A costs $80 (1000).

32-bit DMACs suit 32-bit μCs

The 82258A does not support 32-bit flow-through data transfers but can manage 32-bit fly-by transfers because its address incrementer can count by four. However, many processor-based systems that employ the latest crop of 32-bit μPs require full 32-bit performance from a DMAC. Recognizing this need, Intel Corp currently offers two ICs that incorporate 8-channel, 32-bit DMACs: the 82370 and the 82380. These two devices are companions to the company's 80376 and 80386 μPs. Both chips are 32-bit devices with equivalent features. The address and data buses of the 82370 match those of the 80376 μP and the 82380's buses mate to the 80386 μP. The 82370 (16 MHz) costs $45 (1000) and the 82380 (16 MHz) costs $70 (1000).

The 82370 and the 82380 are not simply DMACs. Their designers also gave them several system-level functions, such as a 20-level interrupt controller, reset logic, a programmable wait-state generator, four interval timers, and a dynamic RAM (DRAM) refresh controller (**Fig 1**). The combination of these components results in a device that offers more performance than you might extract from the individual ICs and saves you precious board space.

Integration breeds performance

Both the μP and the DMAC share the 82370's and the 82380's wait-state generator. The generator lets you create six wait-state settings for your system: three for

DMA basics: flow-through and fly-by transfers

DMA transfers are either flow-through or fly-by. During flow-through (2-cycle) transfers, the DMAC assumes control of the system bus and makes the transfer by acting like a μP. During the first cycle of a flow-through transfer, the DMAC reads a word from the data source and deposits that word in its data register (**Fig Aa**). During the second cycle, the DMAC moves the word from its holding register to its destination. Memory and I/O devices may assume both the source and the destination roles.

During a fly-by (single-cycle) transfer, the DMAC controls the transfer, but the data moves directly from the source to the destination in one bus cycle (**Fig Ab**). The source responds to a read cycle and the destination responds to a write cycle simultaneously.

Processor buses generally do not support simultaneous read and write cycles to two different addresses. Therefore, systems that support fly-by transfers must incorporate special circuitry that allows the DMA-acknowledge-output pin to serve as a second address specifier. The DMAC can select either the source or the destination with its address bus and select the other participant with its DMA-acknowledge pin. Fly-by transfers usually only work between memory and I/O devices. Memory-to-memory DMA transfers must use the flow-through technique.

Because a fly-by transfer moves data from source to destination in a single cycle, it is twice as fast as a flow-through transfer at the same bus speed.

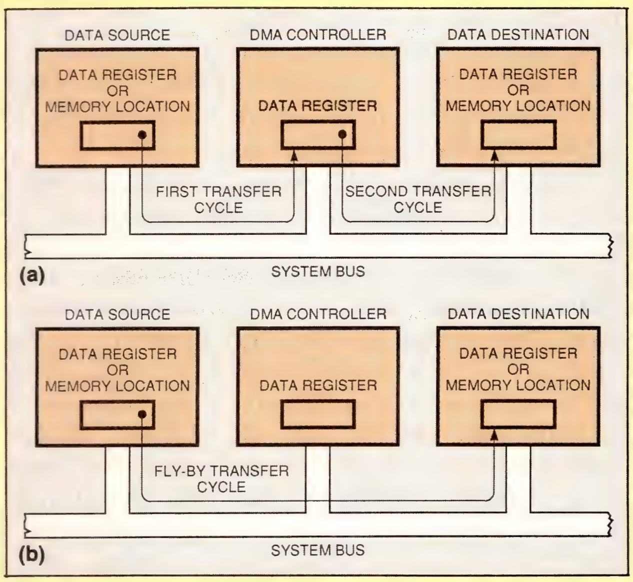


*Fig A—**Of the two types of DMA transfers,** flow-through transfers **(a)** occur in two cycles. During the first cycle, the DMAC reads a word from the data source and deposits the word in its data register. During the second cycle, the DMAC moves the word from the data register to its destination. In single-cycle fly-by transfers **(b)**, the data moves directly from the source to the destination.*

But this extra speed incurs additional cost for the logic that allows a device to respond to conventional bus cycles and to DMA-acknowledge cycles. However, fly-by transfers may make the difference between meeting or missing a system's performance specifications.

DMA controllers

the memory space and three for I/O space. During an access cycle, the device being addressed drives two input pins that select one of the preset wait-state counts. The generator then postpones the cycle's completion by the requested number of counts. The combination of the wait-state generator and the DMAC on one chip eliminates the need to add any additional wait-state circuitry to your system design.

Intel recently introduced a similar device—the 82357 integrated system peripheral—as part of its Extended Industry Standard Architecture (EISA) chip set. (EISA is a specification for an enhanced version of IBM's PC/AT bus. It accommodates 32-bit expansion cards and multiprocessing.) Intel's 82357 incorporates a timer/counter, an interrupt controller, a bus arbiter, and a DRAM refresh controller, in addition to a DMAC, which supports EISA's three special burst-DMA modes. Intel only sells the 82357 with a companion 82358 EISA bus controller. The 2-chip set (25 MHz) costs $99 (1000).

Zilog offers a similar device for its 16-bit μPs—the Z16C20 General Logic Unit. It can control peripheral devices and several types of system memory in addition to performing DMA transfers. The Z16C20 incorporates a 1-channel DMAC, DRAM and static-RAM controllers, a wait-state generator, an EPROM controller that speeds up EPROM accesses by as much as 25%, and two 16-bit timers. One of the timers can also serve as a watchdog timer. The Z16C20's DMAC operates only in the fly-by mode. The device costs $13.33 (100).

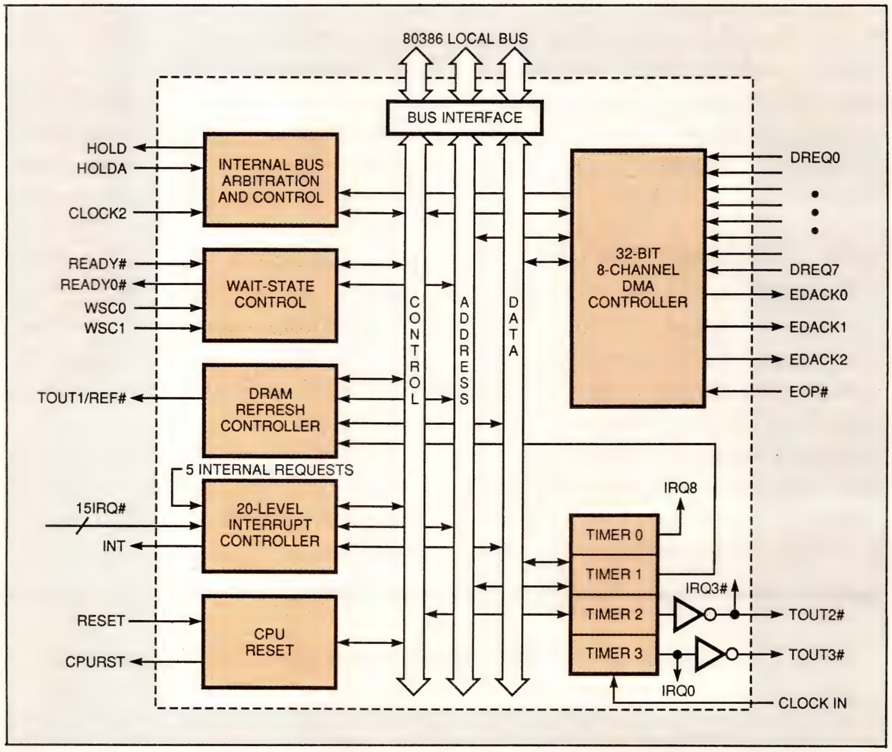


***Fig 1—The combination of a DMAC** and several system peripheral devices on one IC enables the Intel 82380 to provide capabilities that exceed the sum of its parts.*

Merging μPs and DMACs

Intel's 82370, 82380, and 82357 and Zilog's Z16C20 are part of a definite trend in DMAC IC design. Many chip designers are using the bounty of extra transistors, made available by the increasing circuit densities of advanced IC fabrication processes, for additional system functions rather than devoting all their IC's transistors to the DMA controller. To put it another way, many types of ICs now incorporate DMACs. In fact, as **Table 1** illustrates, an increasing number of μPs and μCs include DMACs as part of the processors' basic feature set.

Intel's recently introduced 80960CA μP is an excellent example of a processor with an integrated DMAC. The 80960CA incorporates a 4-channel DMAC in addition to an interrupt controller, a bus controller, and an 80960 processor core. The μP's DMAC is so tightly woven into the fabric of the chip that it shares many of the IC's hardware resources with the processor core. These resources include the integer unit (for incrementing and decrementing registers) and the microcode ROM.

Through a variety of clever design features, the combined abilities of the 80960CA's processor core, DMAC, bus controller, and interrupt controller let the 80960CA achieve better system performance than if these functions were implemented with individual ICs. The interaction between the 80960CA's DMAC and bus controller demonstrates the real power of the combined on-chip functions.

As **Fig 2** illustrates, two 128-bit data buses link the μP's DMAC, bus controller, data registers, and 1k-byte internal data RAM. Because the DMAC and the bus controller use these very wide buses, they can minimize the number of data transfers made inside the IC by packing the data into 128-bit words.

Move 16 bytes per bus cycle

Using only one internal-bus cycle, the 80960's DMAC can perform a 16-byte transfer between the μP's

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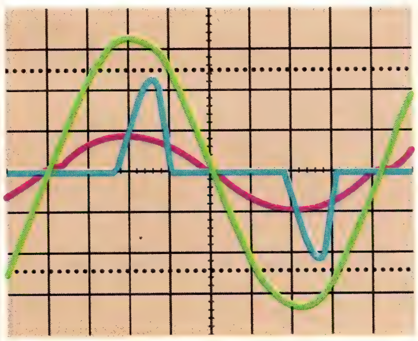

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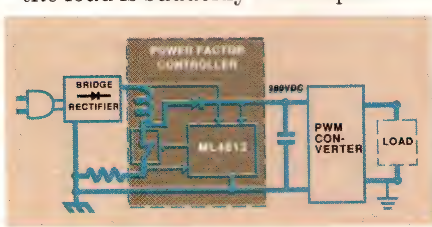

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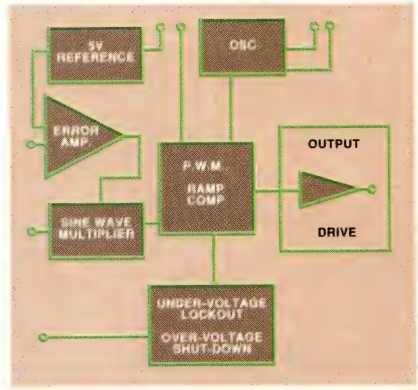

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DMA controllers

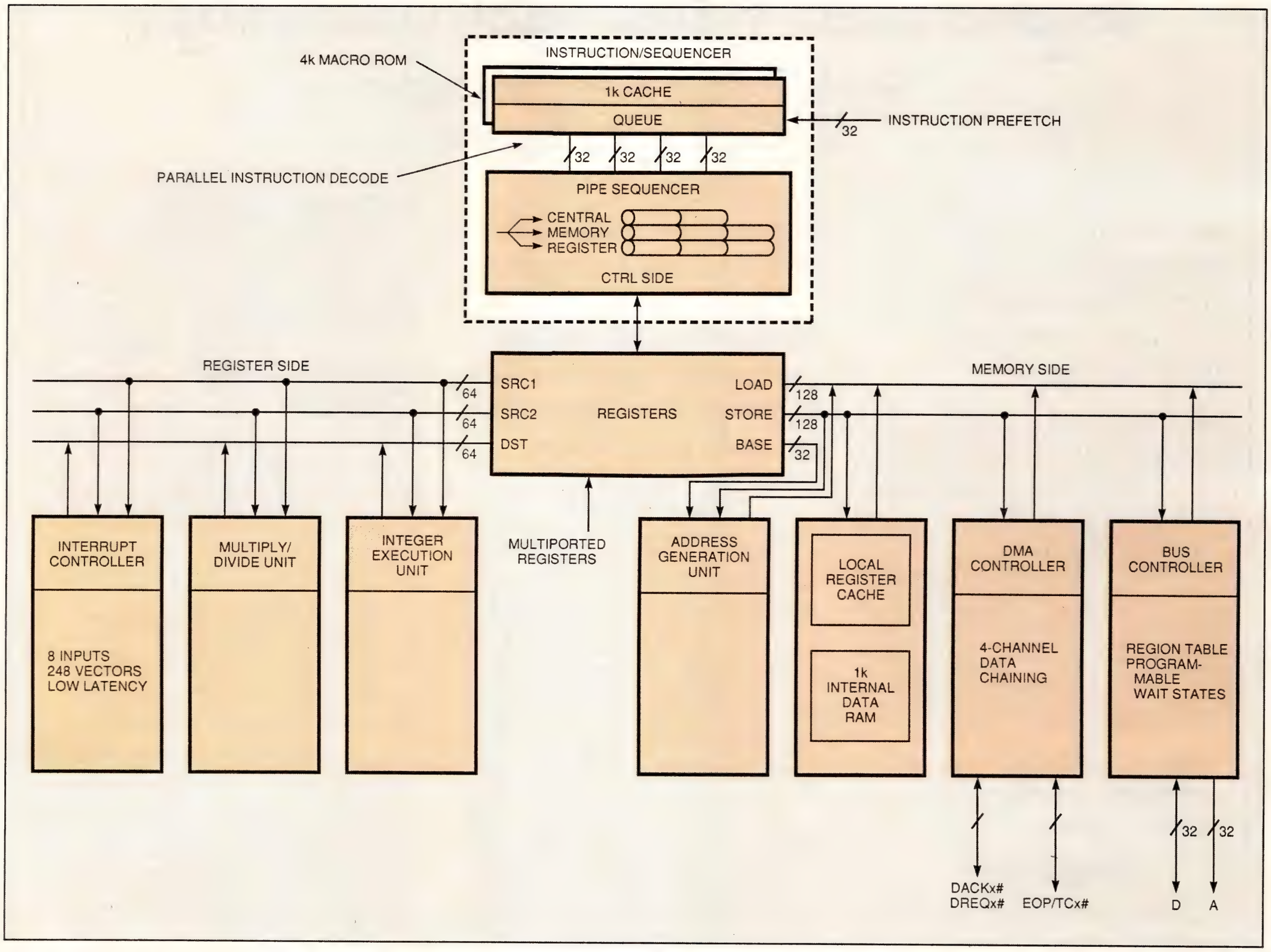

Fig 2—With key system resources on the chip, *Intel's 80960CA μP can move data more quickly than a multichip implementation can. For example, the μP's DMAC can provide data to its bus controller over two 128-bit buses, a capability that saves precious bus cycles in the data-transfer process.*

registers or on-chip RAM and the bus controller. In addition, because there are two of these wide data buses on the 80960CA, the μP's scheduling circuitry never has to turn one of these wide buses around between transfers. Packaging and pin limitations make 128-bit buses impractical as external μP buses, and two such external buses are simply out of the question. But if critical functions are placed on the chip, as they are in the 80960CA, you can employ such a performance-boosting architecture for a 1-chip μP design.

The 80960CA's bus controller uses a memory-region configuration table that lets you partition the chip's address space into 16 regions. For each region, you can specify

- the bus width (8-, 16-, or 32-bit)
- the byte ordering (big-or little-endian)
- whether or not the chip's burst-mode feature should be enabled
- the number of wait states required
- whether or not to use address pipelining. The configuration table specifies how the external bus should operate for transactions initiated by both the processor core and the DMAC.

I/O requests from the 80960CA's processor core and from the DMAC appear nearly identical to those from the bus controller. The μP's scheduling circuitry treats the DMAC as a true coprocessor and intermixes its requests with requests from the CPU in the chip's instruction pipeline. In addition, the processor's instruction set includes two DMA instructions ("set up DMA" and "update DMA") that facilitate construction of fast interrupt service routines. DMA instructions represent just one more example of the enhanced performance that results from building a DMAC into a μP.

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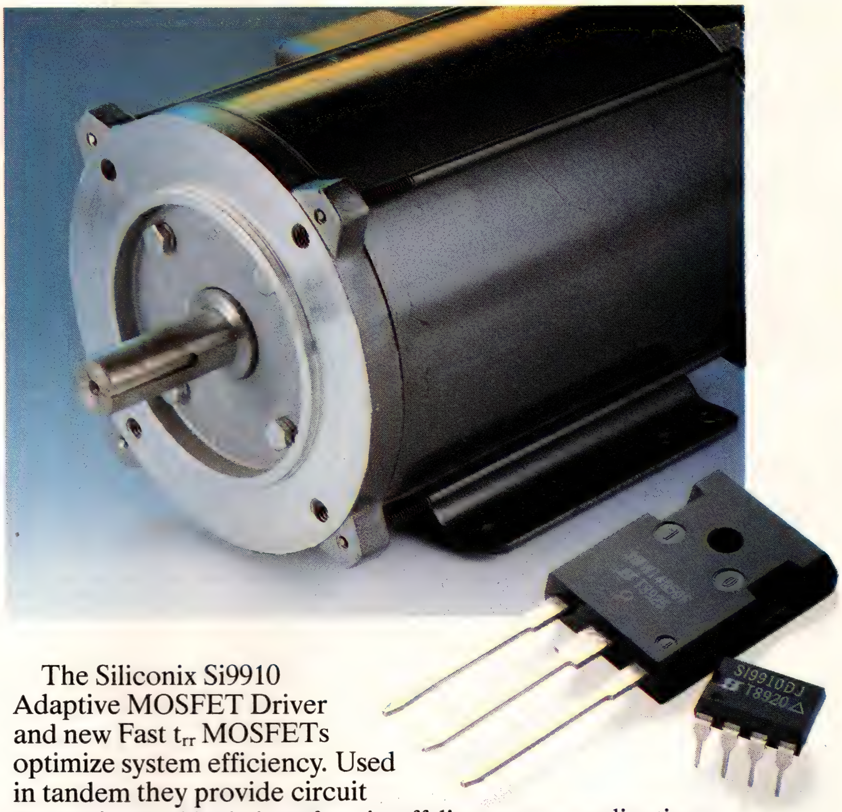

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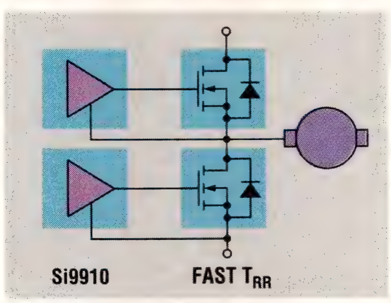

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TABLE 1—REPRESENTATIVE μPs AND μCs WITH ON-CHIP DMA CONTROLLERS

MANUFAC-TURER	MODEL NUMBER	PROCESSOR TYPE	WORD WIDTH (BITS) (SEE NOTE)	DMA CHANNELS	RAM (BYTES)	ROM OR EPROM (BYTES)	CLOCK SPEED (MHz)	PRICE (1000)
HITACHI	HD64180	μP	8	2	NA	NA	6, 8	$6.51 (6-MHz), $7.60 (8-MHz)
	HD647180X	μC	8	2	512	16k	8	$19.10
	H8/532	μC	8	1	1k	32k	10	$42.30
INTEL	80960CA	μP	32	4	1k	NA	16,25, 33	$273 (16-MHz), $303 (25-MHz), $379 (33-MHz)
	83C152	μC	8	2	256	8k	16.5	$12.95 (10,000)
NEC	μPD782XX	μC	8	17	640	0–16k	12	$6 TO $70 (ROMLESS, ROM, ONE-TIME-PROGRAMMABLE, AND EPROM VERSIONS)
	μPD7831X	μC	8/16	8	640	0–16k	16	$12 TO $75 (ROMLESS, ROM, ONE-TIME-PROGRAMMABLE, AND EPROM VERSIONS)
SIGNETICS	68070	μP	16/32	2	NA	NA	10, 12.5	$21 (10-MHz), $26 (12.5-MHz)
TOSHIBA	TMP90C84F	μC	8	11	256	8k	10	$9.50 (5000)
ZILOG	Z180	μP	8	2	NA	NA	6, 8, 10	$8.93 (6-MHz), $10.71 (8-MHz), $20 (10-MHz)
	Z280	μP	8	4	256	NA	20	$28.57 (100)

NOTE: WHEN TWO NUMBERS APPEAR IN THE WORD-WIDTH COLUMN, THE FIRST NUMBER IS THE SIZE OF THE EXTERNAL DATA BUS, AND THE SECOND NUMBER IS THE SIZE OF THE PROCESSOR'S INTERNAL REGISTERS.

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A DMAC can transfer data faster than a CPU operating at the same clock rate because the DMAC is essentially a zero-instruction-set computer. While transferring data, a DMAC uses no bus bandwidth for fetching instructions. In addition, the transfer of bus control between a CPU and a DMAC requires less time than an interrupt context switch does. This situation gives DMA-based I/O transfers even more of a performance edge over interrupt-driven transfers. For the 80960CA, intermixing CPU and DMAC requests in the chip's instruction pipeline completely eliminates context-switching overhead.

However, the performance advantages of integrated, on-chip DMA don't just benefit new 32-bit μPs. You can find integrated DMACs in newer versions of well-established 8- and 16-bit μPs as well. For example, Zilog's Z80 processor architecture serves as the core processor for its Z280 μP and for Hitachi's HD64180 (also available from Zilog as the Z180). Motorola's 68000 μP, a processor with a 16-bit data bus but 32-bit registers, is the core processor for the Signetics 68070 integrated μP. The 64180, Z280, and 68070 μPs all incorporate DMACs, as shown in **Table 1.**

μCs benefit from DMACs, too

Several 8-bit μCs also include integrated DMA facilities. Hitachi's HD647180X, a μC verison of the company's HD64180 μP, replicates the μP version's DMAC capabilities. Other 8-bit μCs such as Toshiba's TMP90C84X series and NEC's 78K2XX and 78K3XX μCs provide a form of DMA controlled by the CPU's hardware.

Block diagrams of the NEC and Toshiba μCs do not show functional blocks marked "DMA controller," but they have DMA capabilities nevertheless. Toshiba calls its DMA operations "micro DMA processing." NEC calls its DMA operations "macro service functions."

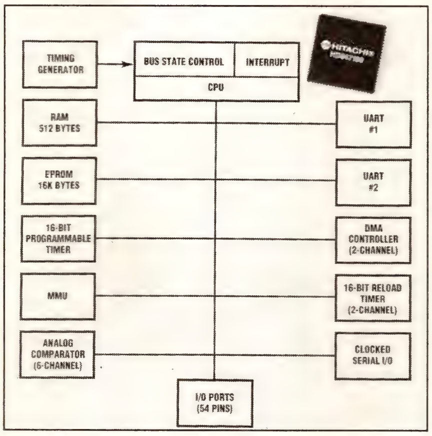
In both NEC's and Toshiba's μC families, the DMA controller circuitry is merged into the processor core. Blocks of μC registers hold source and destination addresses and a terminal count. After a program loads these registers with appropriate values and activates the DMA transfer, the special DMA circuitry in the processor core executes the transfer operation without further program intervention.

NEC has enhanced the macro

DMA controllers

service functions of its 78K2XX μCs, and its DMA operations can often replace quite a bit of software. The μC's type C macro service function accepts interrupts from one of the chip's timers. For each interrupt, the function transfers one byte of data to an I/O port and transfers a new value to the interrupting timer. This enables you to create two tables, one containing data to be output and one containing timer values; the type C macro service function transfers the data using the intervals specified in the timer table.

NEC specifically developed this particular DMA mode to allow the μC to control the ramp-up and ramp-down operations of stepper motors. However, this facility can come in handy when you need to transfer data at irregular intervals.



Typical of the latest μCs, *the HD647180 from Hitachi incorporates a 2-channel DMAC in addition to RAM, ROM, and I/O devices.*

Most processors can only do this through interrupt-service routines, which have relatively long and unpredictable latency times. The 78K2XX-μC family's macro service function treats the job as a background task. In addition, the macro service function is invisible to the μC's program when operating and has a short, fixed, latency time.

Intel's 8XC152 μC family incorporates a 2-channel DMAC to support its high-speed, on-chip, multiprotocol communications controller. This controller can handle several network protocols including synchronous data link control and carrier-sense, multiple access with carrier detection, and it is targeted at high-speed LAN applications.

LAN communications generally involve high-speed transfer rates, and a DMAC helps ensure that the μC can move data from the LAN to memory quickly and efficiently. For example, Ethernet LAN-controller ICs have incorporated DMA capabilities for years. No other

data-transfer technique can support the data rates required by high-speed LANs.

Peripheral chips get DMACs

AT&T recently introduced its T7115, a 32-channel HDLC controller designed for digital T1 and primary-rate Integrated Services Digital Network communications systems. It incorporates a DMAC to handle the demanding data rates required by these telecommunications applications. The T7115 costs \$55 (1000).

DMACs make sense for other serial-I/O protocols, too. Most data-communications protocols employ inherently asynchronous processes that need DMA's low-latency characteristics. For example, Zilog offers two serial devices that incorporate DMACs: the \$75 (100) Z16C30

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For more information on the ICs with integrated DMACs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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universal serial controller (USC) and the $25 (1000) Z16C35 integrated serial communications controller (ISCC). The Z16C30 supports serial data rates up to 10M bps, making it a prime candidate for DMA service. It also incorporates a 32-byte FIFO buffer so that its integrated DMAC can move data from the USC to memory in 32-byte bursts. Burst operation eliminates much of the bus-exchange overhead that occurs between a CPU and DMAC. That overhead can bog down individual DMA transfers.

The Z16C35's two full-duplex serial channels operate at rates up to 4M bps, and its 4-channel DMAC can move data at 3.1M bytes/sec. With two serial channels, each running at 4M bps, the Z16C35 has data-transfer requirements almost as stringent as the Z16C30's.

One of the key benefits of the integrated-DMAC approach is its support for fly-by DMA transfers, which are the most efficient type. Because DMACs are integrated into serial devices, a fly-by DMA transfer involves only two system components (memory and the serial chip) rather than three (memory, the serial chip, and the DMAC). Elimination of the external DMAC also reduces or eliminates the need for additional glue logic.

Integrated DMA controllers require less board space, improve performance, and lower costs. As higher integration levels allow IC designers to redefine existing ICs and invent new devices, you will see an increasing use of DMA to move data in μP- and μC-based systems. For data movement, not even RISC μPs can outperform DMACs.

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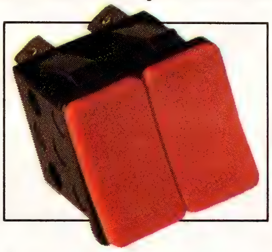

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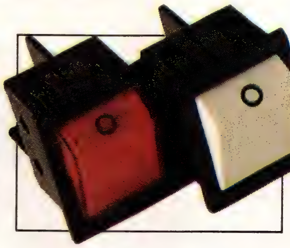

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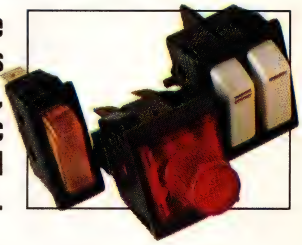

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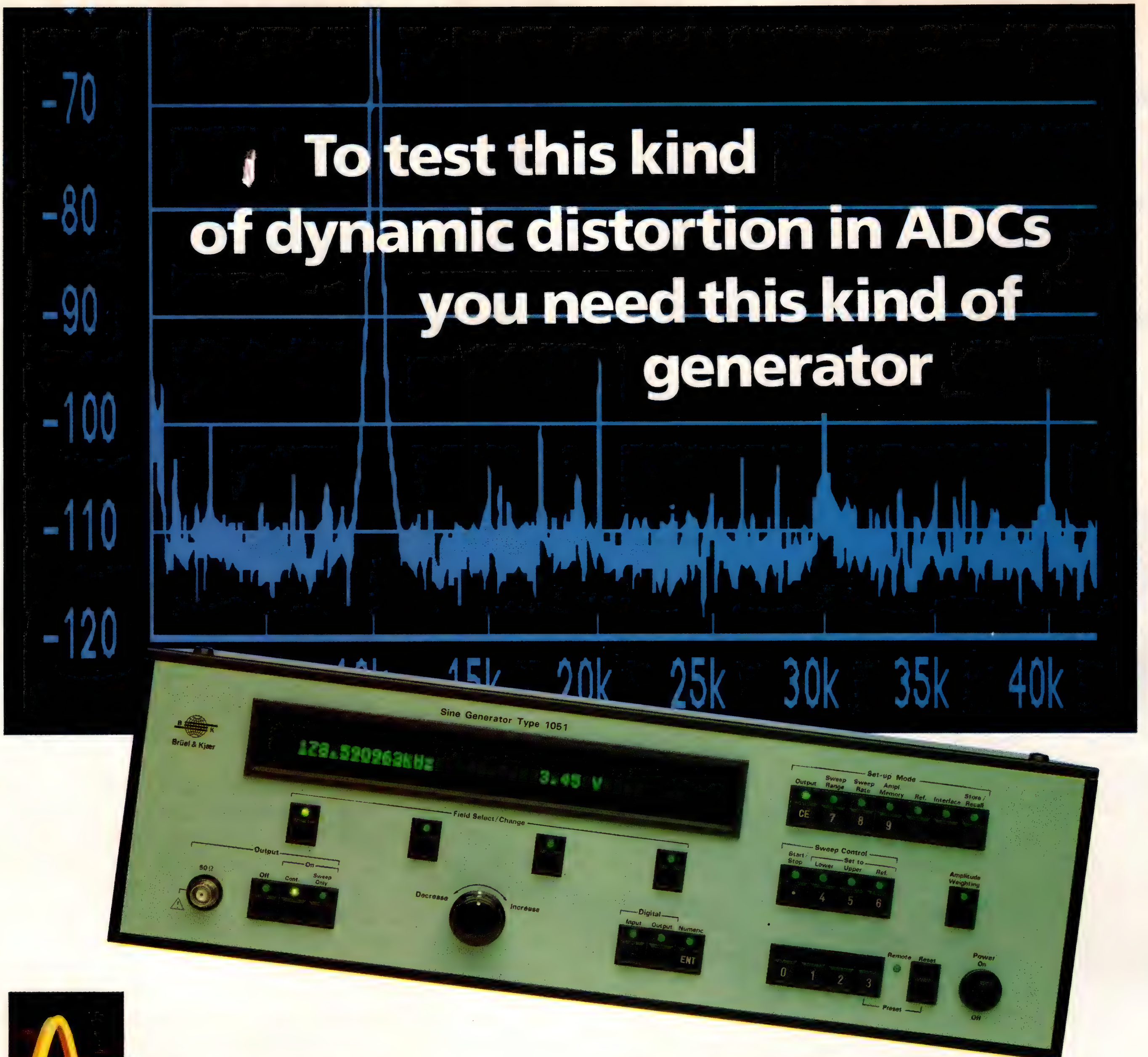

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CAD tools aren't yet on speaking terms

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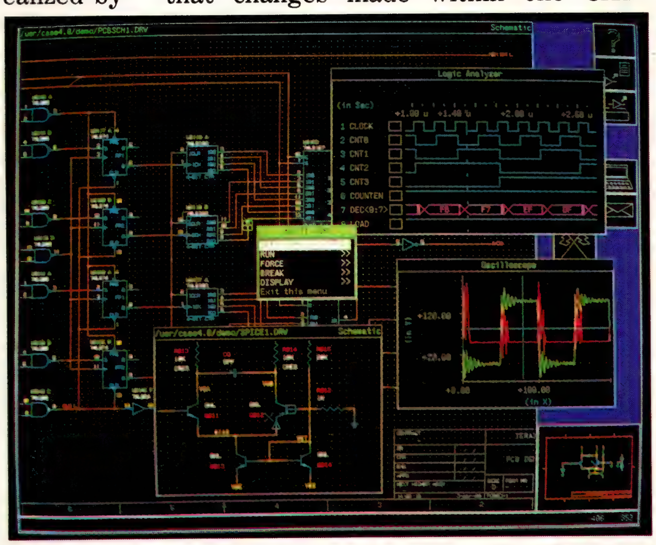
Michael C Markowitz,
Associate Editor

If, like many CAD-literate designers, you've knitted together your own suite of independent CAD tools, you know what a chore the process is. Others, who may be considering adding third-party software to their single-vendor design environment, or who want to customize their CAD workspace, may be in for a rude awakening.

The interfaces between tools from different vendors are akin to the early attempts to develop a railroad system—every company used a different track gauge. Therefore, the advantages gained from using the most flexible logic synthesizer, the most user-friendly schematic editor, the fastest simulator, and other "best" CAD tools can often be lost in transferring your data among the tools. As a result of these inefficiencies, the incremental gains realized by using a CAD tool that is "better" than the one included in your own CAD environment is probably not worth the pain of integration. On the other hand, capability-extending tools that aren't available within your CAD suite may be worth the effort of integration.

Responding to your demands to mix-and-match CAD tools, many CAD vendors are now entering the framework business (**Table 1**). A pleasant, easy-to-conceptualize definition of a framework is a software backplane that allows you to "plug-in" your choice of CAD tools. Through this backplane, the software communicates with the design database and the tools of any other vendor. Unfortunately, the combination of today's lack of framework and design-database standards and the glut of CAD tools and vendors makes the communication among the databases and the various tools range from poor in most cases to excellent in only a few. Andy Graham, design automation systems group manager at Motorola's ASIC Div and president of the CAD Framework Initiative (see **box**, "Initiatives search for CAD framework"), suggests that with today's generation of frameworks, "not having something can be a lower-cost option than having the wrong thing."

Ideally, you want the transfer of information between tools to be so good that changes made within one CAD



Simulation frameworks let you work concurrently *with switch-, gate-, and behavioral-level models, in both the analog and digital modes, on the same design. Unfortunately, very few interfaces currently exist for today's simulators. (Photo courtesy Teradyne EDA)*

Design frameworks

package are automatically made in all the others. For example, as you modify your schematic, your design's corresponding simulation netlist and physical layout would be updated to reflect schematic changes. These mechanical updates would maintain data consistency among your design's behavioral, structural, and physical representations. Such a scenario suggests that you should work with a shared database.

If you do use a shared database, there are two problem areas. The first is that unless the database offers some extensibility, there is no way to allow for the future integration of CAD tools whose features and functions have yet to be defined. The second, which is perhaps more critical from the vendors' perspective, is that investment in their own current tools, databases, and data structures makes vendors reluctant to contribute to a shared database. Despite these hurdles, database sharing does have many attractions.

TABLE 1—REPRESENTATIVE DESIGN-FRAMEWORK VENDORS

FRAMEWORK VENDOR	FRAMEWORK NAME	FRAMEWORK COST	THIRD-PARTY TOOL SUPPORT	INTERFACE COST RANGE
CADENCE DESIGN SYSTEMS	DESIGN FRAMEWORK	$10,000	CALMA, CALMP, DESIGN COMPILER, HILO, HSPICE, SILOS, SPICE, VERILOG	ABOUT $2000
DAISY/ CADNETIX	WORK-SURFACE	INCLUDED WITH APPLICATIONS-DEVELOPMENT KIT $20,000 TO $30,000	ABEL, CALAY, FRAME-MAKER, MAXI, MULTIWIRE, PALASM, PRANCE, SABER, SCICARDS, SMART-MODELS, TEGAS, VISULA	$3000 TO $10,000
FUJITSU	VIEWCAD	$25,000	DESIGN COMPILER, HILO, IKOS HARDWARE SIMULATOR, VANTAGE SPREAD-SHEET, VERILOG	$1000
MOTOROLA	OPEN-ARCHITECTURE CAD SYSTEM	$7500 TO $76,000	DESIGN COMPILER, GED, NETED, QUICKSIM, TANGATE, VERILOG	INCLUDED
SILICON COMPILER SYSTEMS	FOUNDATION	$5000 TO $250,000	HSPICE, MACH HARDWARE ACCELERATOR	$1000 TO $40,000
TERADYNE EDA	VANGUARD	$10,000 TO $20,000	DECSIM, SABER, SMARTMODELS	INCLUDED
VALID LOGIC SYSTEMS	—	NO CHARGE	HILO, LM1000, SABER, SCI-CARDS, SMARTMODELS, SPICE, TEST DEVELOPMENT SERIES, TIGAS, TIMEMILL, VERILOG	INCLUDED
VIEWLOGIC	WORKVIEW	$10,000	ALLEGRO, CADAT, DESIGN COMPILER, HILO, HSPICE, LASAR, POSTSCRIPT, PRECISE, PRISMA, PSPICE, SABER, SCICARDS, SILCSYN, SPICE, SYSCAP, VERILOG, VISULA	FREE TO $40,000

Initiatives search for CAD framework

The CAD Framework Initiative (CFI) was formed at last year's Design Automation Conference. CFI's charter, according to its mission statement ". . . is to develop industry-acceptable guidelines for design automation frameworks which will enable the coexistence and cooperation of a variety of tools." The complexity of CFI's undertaking is emphasized by the seven technical subcommittees that address different areas of the problem.

The Design Methodology group examines and evaluates the operational sequence in which you use CAD tools. The group wants to ensure that when you want to perform a computer-aided operation, the appropriate data is available in the correct format. The Design Representation subcommittee will define a database that is workable within the constraints of today's data structures and models, and is also extensible to support the potential addition of other capabilities.

Such tasks as versioning control, data sharing, data consistency, and storage management fall within the purview of the Design Data Management subcommittee; in short, it protects your team from misusing design data. A User Interface subcommittee is working toward a consistent appearance and behavior for all the design tools. It has also undertaken to specify the procedural interfaces and guidelines for developers and integrators.

To define the links between CAD tools, the Intertool Communication subcommittee will use the work of the Data Representation and Data Management groups to identify and expedite the transfer of objects between tools. The Systems Environments subcommittee is coordinating the User Interface and Intertool Communications groups to define and smooth the boundary between the graphics and operating systems. The Architecture subcommittee will formalize the interrelationships of the different functional areas of the CAD framework and, for consistency, address global frameworks issues.

A similar organization is Engineering Information Systems (EIS), which is Dept of Defense-sponsored

Some commercial CAD tools provide a limited demonstration of the automatic-update capabilities you gain with a common database. The Vantage Spreadsheet from Vantage Analysis Systems (Fremont, CA), for example, updates your VHDL (VHSIC Hardware Description Language) circuit description and the simulation representation when you modify your circuit. Another capability, popular within the home-grown tools of vendors with broad product lines such as Dazix, Valid, and Cadence, is real-time tool communication, whereby you can select a gate in a netlist and have it highlighted in your schematic window.

Instead of intertool communication, what you might get from a framework tying together a diverse set of tools can vary over a wide range. At one extreme of current offerings, the framework can be as simple as a consistent user interface, which gives all the tools the same look and feel—but makes you responsible for ensuring the data compatibility between tools. At the other extreme, some frameworks provide a way of translating information about your design from one tool format to the next.

The translation can be at any of several levels. The most basic level, and perhaps the most popular with the vendors, utilizes a standard interchange format, such as EDIF (Electronic Design Interchange Format) or VHDL. When you want to send your design from one tool to the next, you merely translate your design into one of the standard formats. Motorola's Open Architecture CAD System, for example, uses an EDIF "backplane" that lets you transfer data between tools—as long as they "speak" EDIF.

Unfortunately, these translations eat up lots of time, especially when the tools can't work with the standard formats directly. If they can't, you'll have to run both input and output translations. Also, EDIF, for example, has no allowance for semantics and is therefore subject to interpretation, according to Mike Price, Valid's vice president for corporate engineering and a board member of the CAD Framework Initiative.

An advantage to using standard formats, however, is that a large number of CAD tools currently accept and generate the data in them. And, if you use VHDL as your interchange format, you'll satisfy the Dept of Defense's edict that you document all digital ASICs built for defense contracts by using behavioral and structural VHDL descriptions.

A more advanced level of design-data exchange occurs when the framework vendor couples the tools together so that access to the design data is automatic. Often, access is provided with translators that convert the output data from one tool into the input format for the next. Because you are using a single translation rather than the two-step process of using an EDIF or VHDL intermediary, your run time is reduced.

However, the automatic-transla-

through Honeywell Corp and is focusing its efforts on IC CAD.

Both CFI and EIS have set out to accomplish a goal that should greatly improve your productivity and your ability to choose those tools that best meet your needs. Unfortunately, CFI is an organization of better than 40 companies, all with their own hidden agendas and axes to grind, so progress has been slow. It has taken more than a year for the group to build its structure and to define the scope of the framework problem. Some of its member companies are skeptical about CFI's ability to create order from the chaos; they belong to the organization as much to see where the industry is going as to actually provide a means to integrate your design tools. However, to show its progress, CFI will demonstrate a proposed procedural interface for netlist data between netlist producers, such as editors, and netlist consumers, such as simulators, at the International Conference on Computer-Aided Design (Santa Clara, CA) the week of November 6th, according to Tom Rhyne, CFI's treasurer.

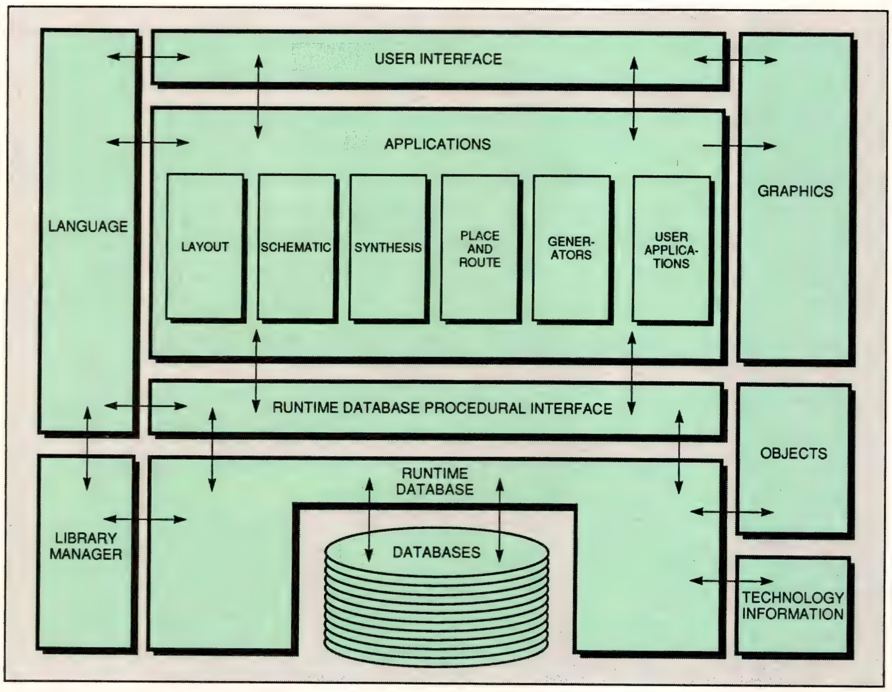
Two potential problems loom: First, to what extent do the two organizations cooperate or compete? To date, they have been cooperative and have expressed the desire not to create conflicting standards. Second, neither organization has considered a formal mechanism to evaluate frameworks and ensure compliance with the standards they hope to define. Independently, Microelectronics and Computer Technology Corp (Austin, TX (512) 338-3521) has announced the creation of the CAD Framework Laboratory to support and evaluate the standards proposed by CFI.

If you'd like to find out more about CFI's efforts, or would like to get involved, circle the reader service number provided at the end of this article or call MP Associates (Boulder, CO (303) 530-4562). For information about EIS, contact Raj Kant, deputy program manager for the EIS program, at Honeywell Systems Inc (Boston, MA (617) 782-7322).

tion process implies that the framework vendor favors a particular design methodology. By creating direct translators between tools, the framework vendors define the sequence in which you'd have to use the tools. One framework, in fact, doesn't integrate the tools; rather, it integrates the design process.

Powerframe, from EDA Systems, is a design-management tool that can work alongside a design-tool framework. It uses an independent database to track tool and file updates, ensuring that you are working with the proper tool and data files. The design-management framework makes no attempt to get other CAD tools to communicate, but it does monitor version tracking and configuration control, data-dependency tracking, design history and status, design-methodology control, and tool sequencing and coordination. In short, Powerframe's purpose is to ensure that your design data is consistent, that you're working with the proper revisions of CAD tools, and that you follow your organization's design methodology.

Some frameworks provide more than just tool integration. *ASICOpen, from Fujitsu, also lets you define a design methodology to assure that you use the correct applications on the proper data in the appropriate order.*



In this framework schematic, *notice that the applications use the procedural interface to communicate with the databases. If vendors can clean up this interface and allow you to plug in your tools, you'll find frameworks much more useful. (Drawing courtesy Silicon Compiler Systems)*

Other frameworks are more concerned with the integration of the various tools; they leave the design-management problem to the designer. For example, though Cadence's Design Framework offers users Cadence's back-end IC design tools mixed with a host of popular front-end tool choices, the framework doesn't perform design-management tasks. Some users suggest that the resulting flexibility gives too much freedom to designers, who may sacrifice documentation to meet tight schedules. What the Design Framework and other tool-integration frameworks do offer is a user-programming language that gives you access to the design database for integrating some of your own tools.

In addition to Cadence, a number of other vendors, such as Viewlogic and Silicon Compiler Systems, already offer similar access. Others, such as Dazix and Mentor Graphics, are planning offerings for early next year. The accesses the first three provide are called procedural-language interfaces because they use

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dynamic-database extraction within either a programming context or a procedure.

Procedural-language interfaces provide relatively close tool integration, but they demand that the tools you want to bring into the framework have the appropriate hooks. To have the hooks, your third-party tool must have been written with the expectation that it would be integrated into your suite of CAD tools; or, you can modify the source code. Of course, there aren't too many CAD packages created with the foresight to anticipate the integration problems, so you'll have to do some coding. To facilitate the process, however, some visionary third-party CAD-tool vendors, including Gateway Design Automation (Lowell, MA) and Synopsys (Mountain View, CA), have written their software with entry and exit hooks that give the framework access to their data structures through procedural-language interfaces. Other vendors are rewriting their tools to add the hooks.

Writing the interfaces isn't trivial. Misha Burich, vice president of engineering at Silicon Compiler Systems, says that "the task [of writing the interfaces] is complicated and must be done by the CAD group." As testimony to the task's complexity, framework vendors such as Silicon Compiler Systems and Valid have organizations in place that will either write the interface for you or consult on the project.

While you wait for the framework and third-party vendors to add the hooks necessary to accept procedural-language interfaces, you have to go through the format and data translators.

Despite the fact that these translators are time-consuming and inefficient, most framework vendors continue to give their users tools that work with them. Valid Logic Systems, for example, currently offers Dial, a Pascal-based language, which lets you write interfaces to its CAD environment.

Even with EDIF- and VHDL-level interfaces and programming tools that help you write tighter in-

Simulation has its own framework

In addition to the general-purpose tool-integration frameworks, both Silicon Compiler Systems and Teradyne EDA have announced frameworks that couple behavioral, logic, and circuit simulators. These tools let you concurrently simulate the same design with multiple simulators. You can perform critical-path analysis with a transistor-level simulator, logic evaluation with a gate-level simulator, and system analysis with a behavioral-level simulator—all while analog simulators look at transistor-, gate-, and behavioral-level interface logic.

The simulation frameworks offer both historical and forward-looking advantages over integrated, multilevel, mixed-mode simulators like Analogy's Saber or Silicon Compiler Systems' Lsim. On the one hand, you protect your investment in your models and previous design work. If you've accumulated a large collection of Spice models, for example, you can use those existing models with your simulator within these simulation frameworks, rather than redevelop the models for an integrated simulator. On the other, if you need to incrementally add some simulation capabilities in the future, the simulation frameworks will coordinate the processes.

A controller or manager monitors all of the simulators and takes responsibility for all of the critical coordination functions. These functions include the sharing of the common circuit representations, the parceling out of the appropriate pieces to the right simulator, and the synchronization among event-driven, timing-based, and compiler-based simulators.

The problem with adding multiple concurrent simulators to your design arsenal is that you run into an interface problem like that faced in trying to integrate different design tools into a CAD environment. An added wrinkle in the simulation-framework problem is that in addition to exchanging data, the tools must also work synchronously. Such added complexities increase the integration cost. Teradyne's Joe Lassiter estimates that it has taken about six man-months for other vendors to write the interfaces to Teradyne's simulation framework.

As with general-purpose frameworks, the dearth of available interfaces limits the current usefulness of the simulation frameworks. If you use simulators from Silicon Compiler Systems, Teradyne, or any of the few other simulators that already have interfaces written for them, then the simulation frameworks will probably work for you. Otherwise, as with frameworks in general, the benefits you'll realize from simulation frameworks are probably, at best, a year or two away.

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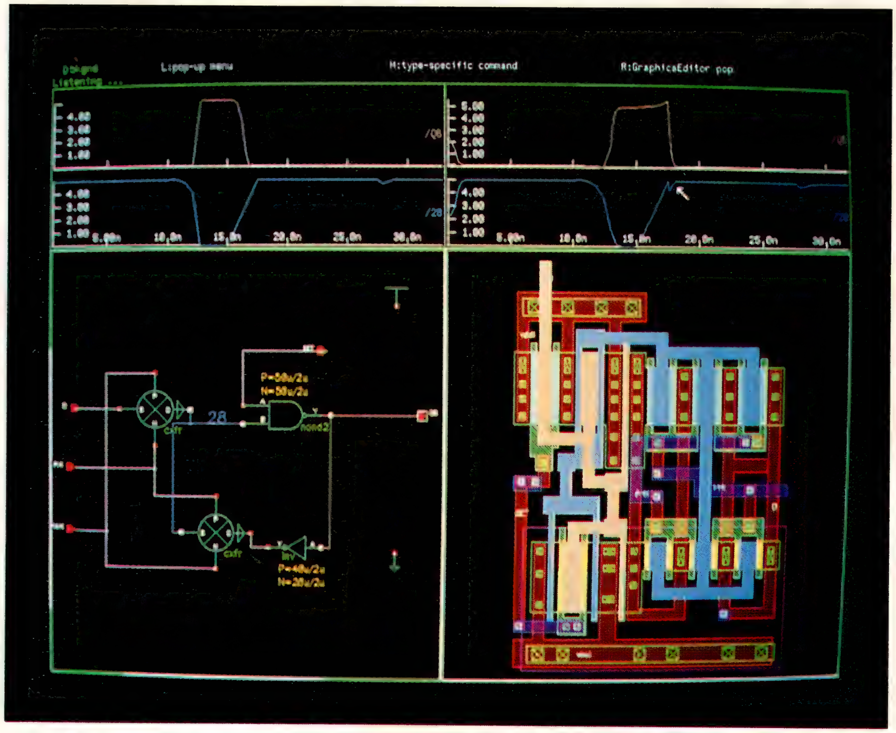
Design frameworks

terfaces, CAD users aren't satisfied. Tom Abels, a CAE applications support engineer at Magnovox, says that the company has resisted buying a commercial framework to organize its diverse collection of CAD tools. Instead, it developed its own framework. With all of its users free to choose whatever software they want, no commercial framework gives Magnavox any greater flexibility than the one it developed internally at a competitive price.

Solbourne Computers, which makes Sun-compatible workstations, has had a similar experience. Though it is constantly evaluating commercial frameworks, its need for the highest performance CAD tools has made framework-vendor cooperation and commitment critical. The company wants to buy a framework that will allow it to use the best tools without the company having to write translators or inter-



***Ideally, you'd like to modify your schematic based on the results of a simulation** and have your layout automatically updated to reflect the changes—all without having to jump from one application package to another. (Photo courtesy Cadence Design Systems)*

For more information . . .

For more information on the computer-aided-design frameworks discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Design frameworks

faces. "The vendors are making lots of noise about frameworks, but they seem to have a low willingness to commit. They'd like to let the first or second guy make all the mistakes, then they can learn from the other guys' mistakes and be the cavalry riding over the hill," says Dan Ganousis, an ASIC design engineer at Solbourne.

There are companies, though, that have adopted commercial frameworks. Senior CAD Engineer Dwight Klaus explains Microchip Technology's decision to use the Cadence Framework as largely the result of Microchip already using most of Cadence's tools. However, instead of the simulators Cadence offered, Microchip wanted to bring Zycad's Mach simulator and Silicon Compiler Systems' LSIM into its environment. Klaus found the process of going through Cadence's interpreted-interface language, Skill, to be both time-consuming and painful. He estimates it took his CAD group three to four man-months to create the Mach interface, but once they learned some programming tricks, they cut the time in half for the LSIM interface. However, his group is still refining, debugging, and enhancing the interfaces. Worse, maintenance activities consume up to 20% of his time. And even with the interfaces, Klaus figures that Microchip's simplest designs require 15 minutes to feed through the translators—and the process slows considerably with increasing circuit complexity.

Users aren't the only unhappy ones. Some third-party CAD-tool vendors are worried that the framework vendors' hearts aren't in the right place. According to Shawn Hailey, president of Meta-Software, "Because they make money selling the interfaces, most [framework] vendors are more motivated selling a disorganized set of interfaces than a cohesive set of tools." In addition, Meta-Software has found that framework vendors can design an interface for their own tools at whatever level they want, but third-party vendors have found the playing field tilted.

Meta-Software has encountered resistance to its efforts to develop the front end for its software. The resistance might be an attempt to protect a framework vendor's proprietary database or a move to favor the vendor's competing tool, but the company wonders whether a CAD user's proprietary tool might face the same obstacles.

If you've already constructed your own design framework, then the current generation of framework tools probably doesn't offer you anything you don't already have. On the other hand, if a broad-line CAD vendor or silicon supplier selling CAD tools offers most of the tools you need, then integrating one or two tools might be a worthwhile, though far from trivial, undertaking. And, if you want to integrate popular tools and you have some leverage, you might negotiate having the CAD supplier build the interface—but don't be surprised if he turns you down.

As with the first generation of most CAD tools, the sizzle promises more than the steak delivers, but "it's important to remember that frameworks are an evolving technology," says Kathleen Barry-Albertini at Harris Scientific Calculations. Whereas these frameworks may not provide you with the capability you need today, they ultimately should develop into a powerful tool that will give you much greater design flexibility. EDN

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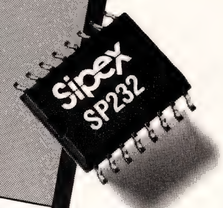

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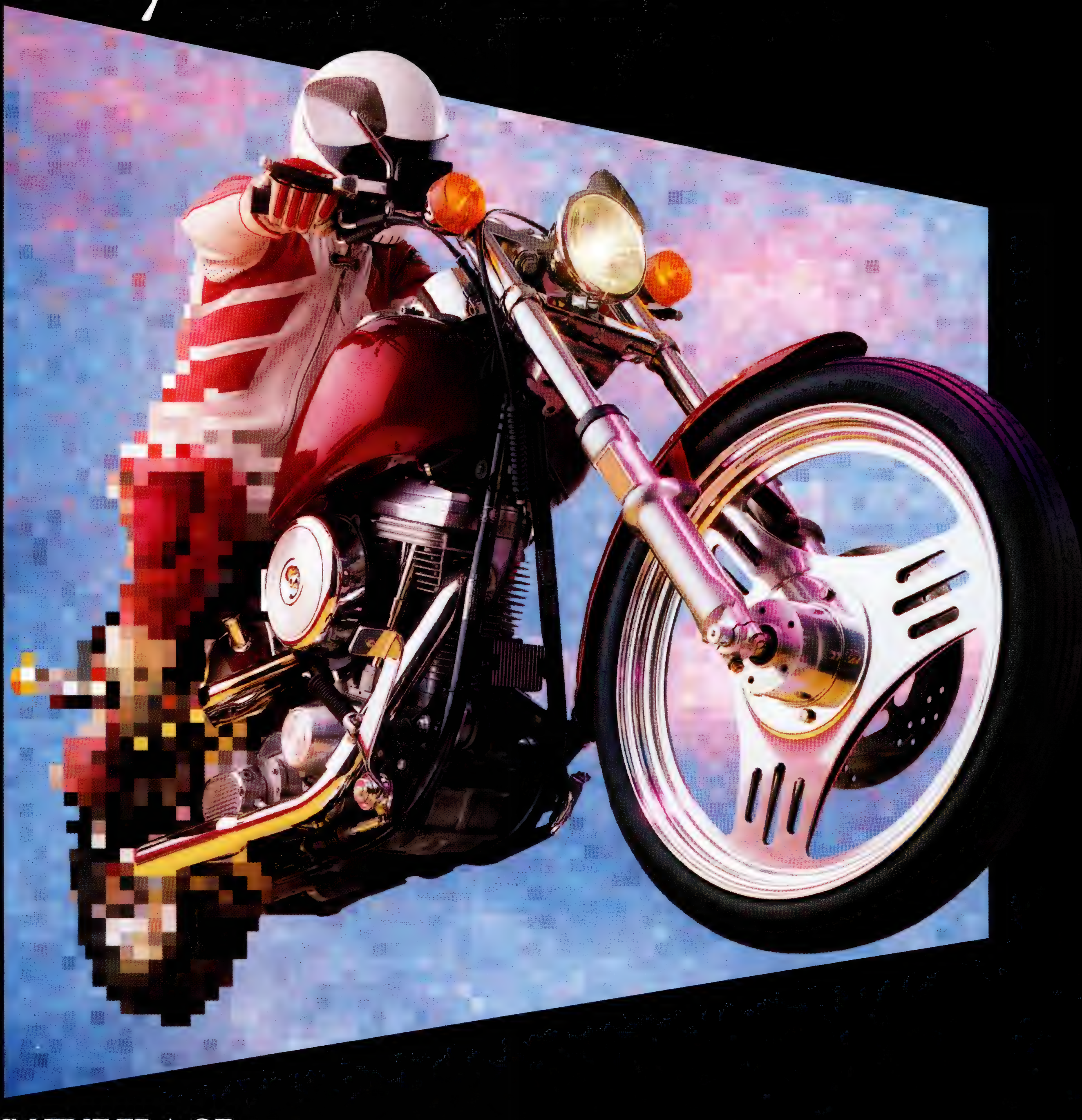

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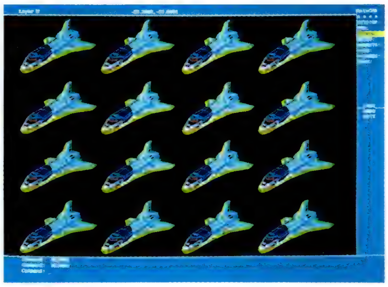

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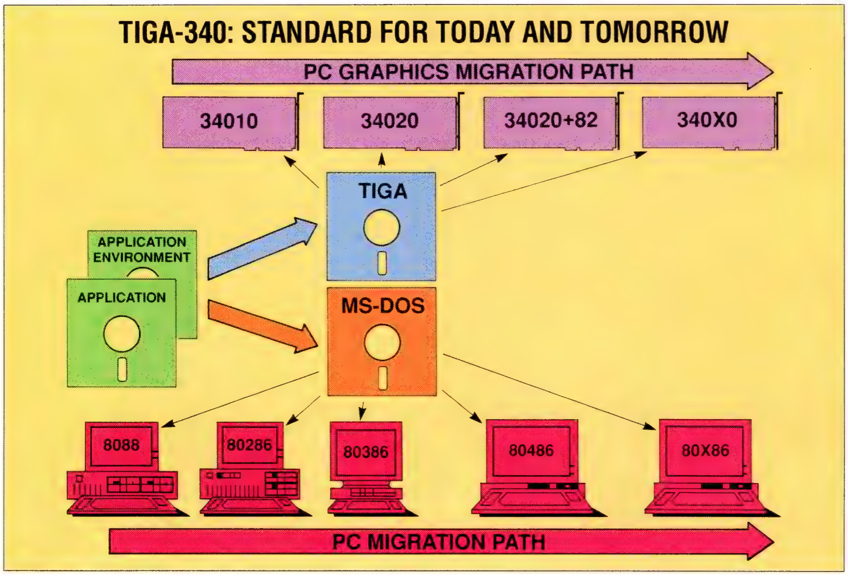

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Applications portability

TIGA allows an application to be ported to a wide variety of 340-based graphics systems with a single software driver. Applications will run without modification regardless of resolution, color content, or specific 340 family processor.

For example, the Microsoft® Windows driver, which is part of the TIGA Software Porting Kit (*see next page*), allows Windows to run without any change on boards having resolutions from 640 x 480 to 4096 x 4096 and color content from monochrome to 256 colors or more.

Speeds time to market

Now hundreds of popular applications can be made available for your new graphics product almost instantly using TIGA and Microsoft Windows. Porting TIGA to a 340-based board typically takes less than one man-week of effort.

More than 150 OEMs have made the TMS340 graphics family their own. That wide acceptance, coupled with open architecture and a defined migration path, makes the future for TIGA-340 and the TMS340 family rich and promising.

A PERSPECTIVE ON GRAPHICS INTERFACE STANDARDS

TI's leadership TMS340 graphics family

No other supplier comes close to TI in the range of cost/performance options for the development of integrated graphics solutions. The widely used TMS34010 processor and other family members are now

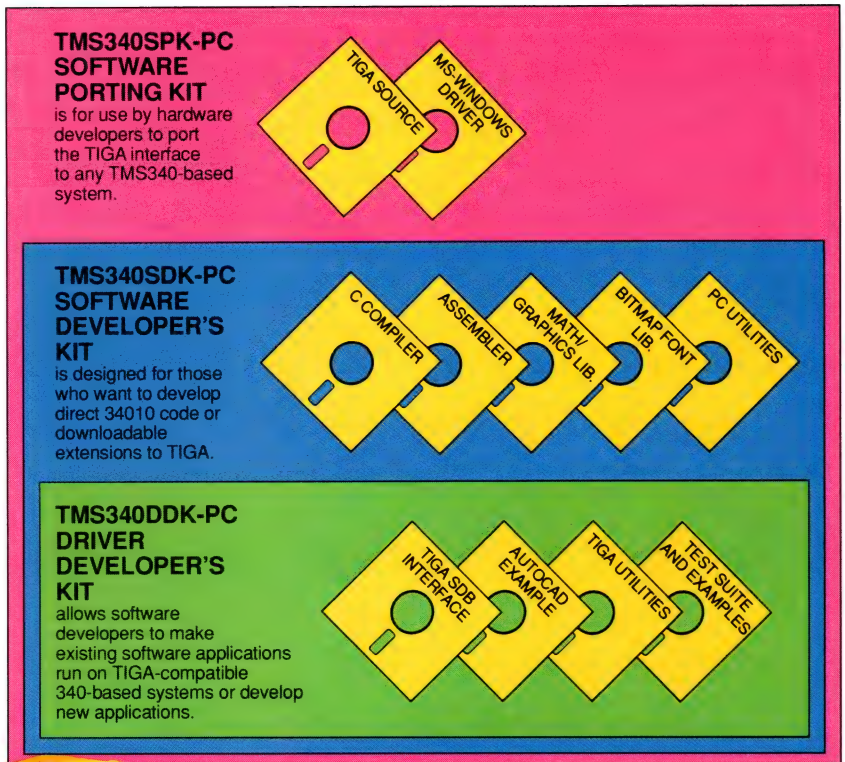
being joined by a group of new-generation products that will bring the higher levels of workstation performance to PCs.

Chief among these is the TMS34020, a programmable, 32-bit processor up to 20 times faster than the 34010.

For use with the 34020, the TMS34082 will perform floating-point operations up to 100 times faster than current PC coprocessors. It is the industry's first graphics floating-point coprocessor.

The family's video RAMs, invented by TI, have been augmented by the TMS44C251 1-megabit VRAM. It was designed in conjunction with the 34020 for the high system bandwidths demanded by today's mid- and high-resolution graphics systems.

TIGA-340 DEVELOPMENT KITS



Free user's guide

For more information about the TIGA-340 standard, get your free copy of the *TIGA-340 Interface User's Guide* and the *TIGA-340 Interface Brochure*.

Call 1-800-336-5236, ext. 3526, or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

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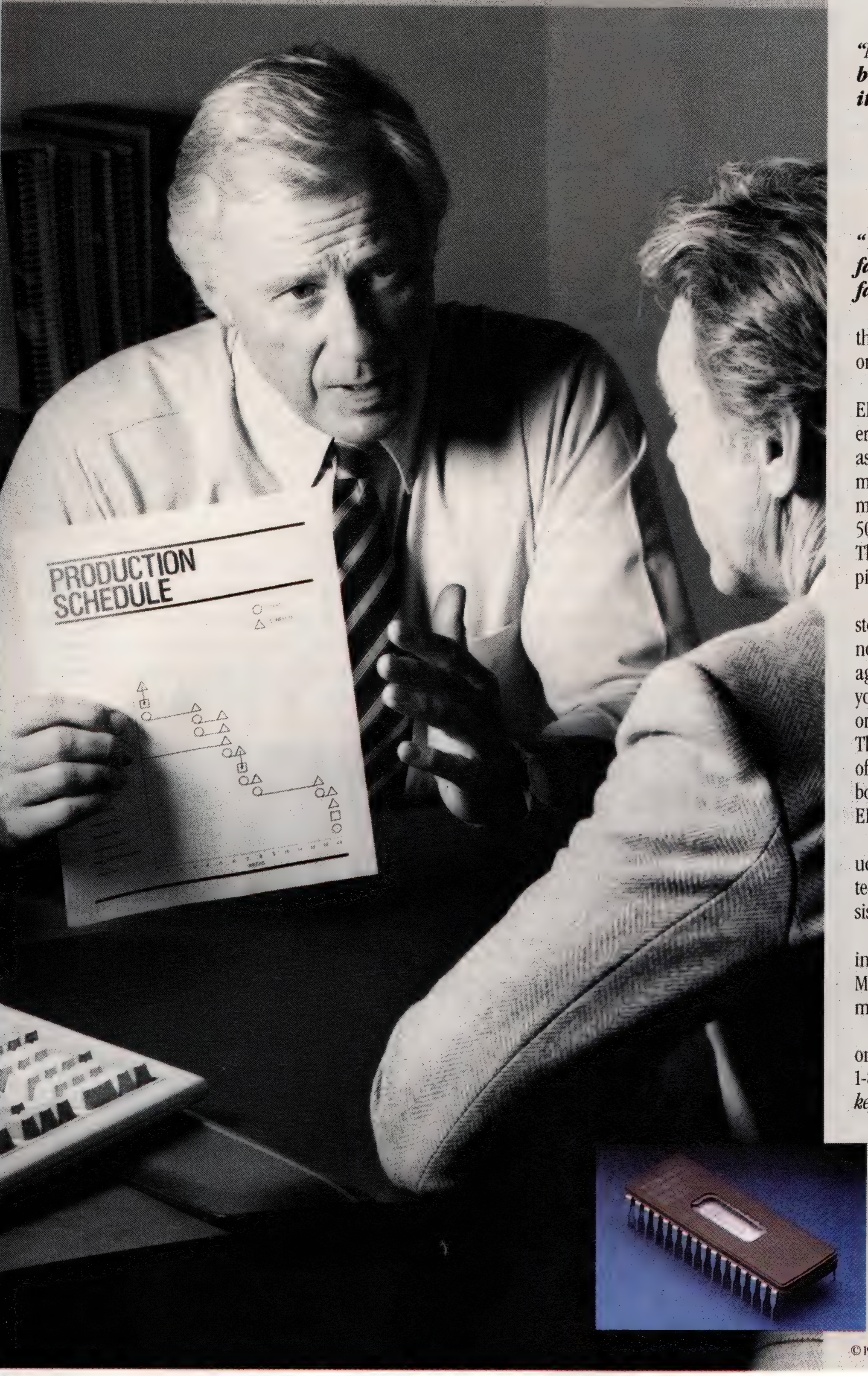

"They're the fastest way to get us from finished design to finished product."

"The 4Mb density means we can increase program storage."

"Not only that, it improves reliability by reducing parts count. And it reduces system power demand."

"Plus, the high-speed programming mode cuts programming time. To about 1/5 the time-per-byte of a 1Mb EPROM."

"They're JEDEC standard, they're fast, and Toshiba can deliver them fast."

If your designs call for multiple EPROMs, these devices are just what the designer ordered.

They're 524,288 word by 8 bit CMOS EPROMs, electrically programmable and erasable by ultraviolet light. They access in as little as 150 ns. The high speed programming mode reduces programming time to 10 microseconds per byte. And they draw only 50 ma at 6.7 MHz. Only 100μa on standby. They come in a 600 mil JEDEC standard 32-pin cerdip package.

Whatever your microprocessor program storage application—operating code, diagnostic software, even standard software packages—these advanced EPROMs will give you a real design advantage. Their byte-wide organization makes them ideal for the job. The 4Mb density cuts cost-per-bit over the life of the system. And the 4Mb EPROM saves board space by reducing the number of EPROMs required.

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 CIRCLE NO 115

Current technologies go on stage at Wescon

The City by the Bay is the venue for the 38th annual show, where you can evaluate products, polish your technical knowledge, make contacts, and keep up with current trade issues.

Kathleen Vejvoda,
Associate Editor

San Francisco's Moscone Convention Center and Brooks Hall/Civic Auditorium complex will be the scene of Wescon/89 from November 14 to 16. During the 3-day event, you can view 1200 exhibits of electronics wares and attend technical-study sessions. More than 1000 companies will display and demonstrate products such as electronic-design and -automation tools; test, measurement, and inspection tools; semiconductors and other components; and production equipment. Also, you can attend a wide selection of technical sessions focusing on design and manufacturing topics.

The show will introduce Autonet, a multivendor network of circuit-design and -test software and equipment. This exhibit will take you through the complete design cycle of a functional pc assembly and show you how each element in this networked, CAE/CAD system contributes to the development of a typical electronic product. In addition, a special section of the show floor—the Automated Design Center—will feature demonstrations of automated-design tools and engineering workstations.

Another exhibition highlight is the microwave/RF product section, which will be located in Brooks Hall. This section of the show floor will display products such as amplifiers, attenuators, connectors, filters, mixers, oscillators, switches, and test equipment.

When you're not visiting exhibit booths, you can attend any of more than 50 technical sessions and short courses. This year's hot technical-session topics include neural networks; video-systems technology; 32-bit embedded controllers; VHDL (the VHSIC hardware-description language); and the high-definition-television systems that have been proposed for the new FCC standards.

Wescon offers two special sessions on neural networks. **Session 33** will discuss what is needed to make this fault-tolerant technology commercially viable. The session will focus on how to start using neural networks for real applications, and a special presentation will explore the research and use of neural networks in Europe. **Session 29** will report on the latest neural-network applications, including communications, robotics, and military applications.

Video-systems technology in imaging, entertainment, and communications is the subject of **Session 21.** The session will include a look back at 50 years of video systems and a look ahead to emerging trends in interactive media systems. Other papers will discuss desktop video

Photography courtesy of San Francisco Convention and Visitors Bureau

systems and the evolution of global standards for high-definition television. (If you're interested in high-definition television, a presentation on possible systems for this technology will take place each day of the show from 9 to 11 am.)

If you enjoy a healthy debate about design tactics, you can attend **Session 26,** in which representatives from Motorola Corp and Intel Corp will each present their com-

WESCON/89 TECHNICAL SESSIONS

		MOSCONE CENTER			CIVIC AUDITORIUM	MERIDIEN HOTEL
TUESDAY, NOVEMBER 14	8:30 AM–10:30 AM	**SESSION 1** A NEW GENERATION OF ECL CIRCUITS SHATTER SYSTEM PERFORMANCE BOTTLENECKS	**SESSION 2** INTELLIGENT MEMORIES PROMISE PRODUCT AND MARKET NICHES	**SESSION 3** ARCHITECTURAL IMPLICATIONS OF ASIC TECHNOLOGIES	**SESSION 4** CAD FOR MICROWAVE CIRCUITS	
	12:30 PM–2:30 PM	**SESSION 5** ADVANCED LOGIC — MEETING SYSTEM DESIGNER NEEDS	**SESSION 6** SPECIALTY MEMORIES: COST EFFECTIVE SOLUTIONS TO HIGH PERFORMANCE SYSTEMS	**SESSION 7** DESIGN METHODOLOGIES FOR BRIDGING THE 1–100K GATE ASIC SPECTRUM	**SESSION 8** ACTIVE MICROWAVE DEVICES	
	4:00 PM–6:00 PM	**SESSION 9** SILICON INTEGRATED CIRCUIT SENSORS AND MICRO-STRUCTURES	**SESSION 10** CONTENT ADDRESSABLE MEMORY (CAM) APPLICATIONS FROM PATTERN RECOGNITION TO LAN BRIDGING	**SESSION 11** RISC — THE NEXT GENERATION	**SESSION 12** COMMERCIAL APPLICATION OF GaAs IC AND SILKICON MMICs	
WEDNESDAY, NOVEMBER 15	8:30 AM–10:30 AM	**SESSION 13** JTAG/IEEE SERIAL PROTOCOLS REDUCE THE DESIGN CYCLE AND IMPROVE TESTABILITY, MANUFACTURING AND FLEXIBILITY	**SESSION 14** **SPECIAL SESSION** VHDL — A STANDARD HARDWARE DESCRIPTION LANGUAGE FOR CAD/CAE/CAT	**SESSION 15** THE INCREASING SOPHISTICATION OF ELECTROMAGNETIC COMPATABILITY (EMC)	**SESSION 16** ADVANCES IN SIGNAL PROCESSING	**SESSION 17** USING COMPUTER AIDED ENGINEERING TO VERIFY DESIGNS
	12:30 PM–2:30 PM	**SESSION 18** AI/EXPERT SYSTEMS	**SESSION 19** COMPUTER AIDED SOFTWARE ENGINEERING (CASE) TOOLS — IMPROVING PRODUCTIVITY	**SESSION 20** AUTOMATIC CONTROL AND CIM IN SEMICONDUCTOR MANUFACTURING		
	1:00 PM–4:00 PM				**SESSION 21** **SPECIAL SESSION** VIDEO SYSTEMS TECHNOLOGY: EVOLUTION OR REVOLUTION?	**MARRIOTT, ROOM SUNSET A** IEEE REGION 6 STUDENT PAPER CONTEST
	4:00 PM–6:00 PM	**SESSION 22** TEST AND MEASUREMENT APPLICATION SOFTWARE FOR THE PERSONAL COMPUTER	**SESSION 23** DEVELOPMENT TOOLS FOR RISC EMBEDDED CONTROLLERS	**SESSION 24** PC BOARD PROTOTYPES FOR $60 IN 60 MINUTES	**SESSION 25** FUTUREBUS +	
THURSDAY, NOVEMBER 16	8:30 AM–10:30 AM	**SESSION 26** **SPECIAL SESSION** 32-BIT EMBEDDED CONTROLLER	**SESSION 27** HIGH PERFORMANCE. COST EFFECTIVE FIBER OPTIC SOLUTIONS FOR DATA COMMUNICATION APPLICATIONS	**SESSION 28** DISTRIBUTED POWER FOR THE NINETIES		**SESSION 29** **SPECIAL SESSION** NEURAL NETWORKS FINAL APPLICATIONS
	12:30 PM–2:30 PM	**SESSION 30** SOFTWARE FOR RISC ARCHITECTURES	**SESSION 31** **SPECIAL SESSION** FLAT PANEL INFORMATION DISPLAYS	**SESSION 32** APPLICATIONS OF ADVANCED RECHARGEABLE BATTERIES FOR PORTABLE POWER		**SESSION 33** NEURAL NETWORKS IN THE REAL WORLD

pany's competitive solutions to high-level, high-performance embedded-system design. Other companies will present papers on embedded applications and on development tools for embedded 32-bit systems. This special session will convene on Thursday, November 16, at 8:30 am.

Papers in **Session 14** will delve into designing, modeling, and testing with VHDL. In addition to the technical sessions, you can attend any of 19 short courses, which will cover, among other topics, modern microwave semiconductor devices, optics and computing, and environmental-stress screening. The technical sessions will be held at the Moscone Center, the Civic Auditorium, or the Meridien Hotel, and all short courses meet in the Civic Auditorium. You must pay a fee for any short courses you wish to attend.

A conference entitled "Economic Forecast for 1990 and Beyond" will examine the impact of the economy on the electronics and computer industries. Many visitors are likely to be interested in the special panel discussion "Europe 1992" on Tuesday, November 14, which will address the implications for American companies of the 1992 EEC accords. All conferences require a fee.

For more information on Wescon, call Electronic Conventions Management at (213) 772-2965. Also, watch for EDN's extensive coverage of Wescon product exhibits and technical sessions in the next issue.

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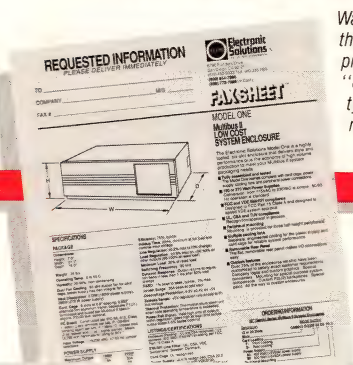

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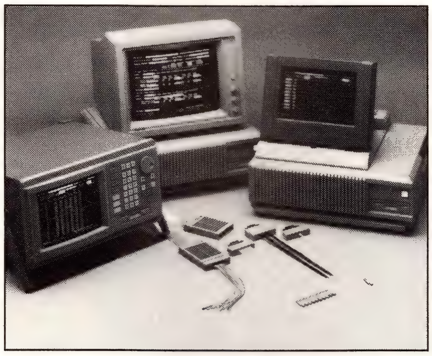
CIRCLE NO 116

Logic analyzer triggers on hardware faults to 2 GHz

The Prism 3001HSM hardware-analysis logic analyzer is the newest member of Tektronix Inc's recently introduced Prism 3000 family. By using a group of "leadsets" (units that everyone but Tektronix would call pods), you can tailor the 3001HSM's capabilities to your needs. The analyzer also lets you establish trigger conditions based on the way you think about hardware problems. For example, the 3001HSM will trigger directly on setup times that violate limits you specify or on pulse durations narrower than a value you supply. All told, the 3001HSM can test for 15 fault conditions. Customarily, logic analyzers do not trigger directly on faults; triggering must conform to restrictions imposed by the instrument.

With the appropriate leadset, the analyzer can acquire data asynchronously at 2 GHz on four channels and store 12k words of data. If you choose a leadset with a maximum asynchronous acquisition rate of 400 MHz on 20 channels, the unit uses transitional timing to effectively increase its memory depth. For state analysis, the instrument can acquire data synchronously on 18 channels at 300 MHz, a figure that drops to 200 MHz during dual-threshold acquisition, a mode useful for spotting marginal amplitude conditions. You can also add leadsets that digitize two analog waveforms to 11 levels (3½ bits) at 400M samples/sec. Because the leadsets are external to the logic analyzer, you can rapidly reconfigure the system.

The heart of the instrument is a large pc card, the 30HSM. As many as ten 30HSM boards can plug into the company's Prism 3002 series of modular logic-analysis systems to give the systems a capacity of 200 fully time-aligned channels. The 30HSM costs $6500; the 3001HSM carries a base price of $11,000. Leadsets range from $900 to $2400. Delivery is eight weeks ARO.



***Plug-in "leadsets"** allow you to quickly reconfigure the Prism 3001HSM high-speed hardware logic analyzer. As many as 10 30HSM boards (the 30HSM forms the heart of the stand-alone 3001HSM) can plug into the expandable system units of the 3002 series to provide 200-channel capacity.*

—Dan Strassberg

Tektronix Inc, Box 12132, Portland, OR 97212. Phone (800) 426-2200.

Circle No 731

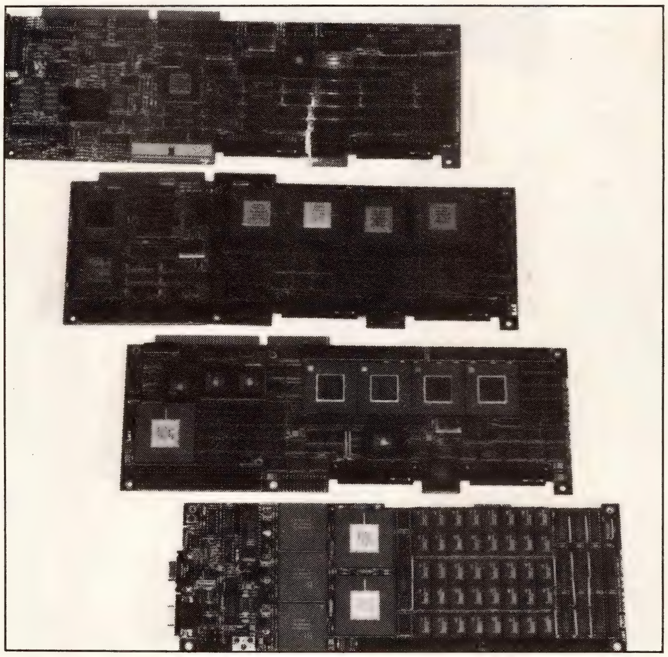
1280 × 1024-pixel image-processing boards run at 30-MHz bus speeds

Your IBM PC/AT or compatible computer can now perform real-time image processing and acquisition at display resolutions reaching 1280 × 1024 pixels. All you have to do is plug in a set of four boards collectively referred to as the Image Series. The four boards include the IM-1280 base board, the IM-RTP real-time processor board, the IM-CLD color-acquisition board, and the IM-ASD asynchronous slow-scan and high-resolution acquisition board. These boards communicate via a proprietary 32-bit dual-bus expansion interface that provides a data rate of 30 MHz.

The IM-1280 base board performs system and display control by means of a resident 10-MIPS, 32-bit TMS34020 graphics processor that serves as a local CPU. Accordingly, this intelligent controller handles the communications among the Image Series boards without monopolizing the host's CPU. An address generator provides independent processing and display addresses for concurrent data display and manipulation; thus, the board provides flicker-free displays even while performing data transfers and operations.

The base board uses a pipelined architecture to maximize system throughput. A software set of more than 200 graphics and image processing functions resides on the IM-1280 to cut development time. Referred to as the Core code, these functions include convolutions, statistics, measurements, and recursive morphology. For intense number-crunching, you can add a 40M-flops TMS34082 floating-point unit.

The IM-1280 contains four 1k × 1k × 8-bit frame buffers that you can stack for true-color image processing. The base board also has a separate 2k × 1k × 4-bit overlay buffer, thereby allowing you to create complex graphics-and-image compositions.



This 4-board set uses a 32-bit graphics CPU *to provide a sustained serial-processing rate of 50 frames/sec for real-time point-to-point transforms and spatial filtering.*

Additional host-based software libraries and drivers come with the Image Series to further reduce application development time and to simplify system integration. Standard libraries include support for such user interfaces as X-windows and Presentation Manager. You also receive a command-line interpreter, a configuration program, and a diagnostics program.

The IM-RTP real-time processing board performs such functions as interimage manipulation, point-to-point transforms, statistics, and morphology analysis. Images can come from a live video input or a frame buffer. Or the board can combine live and stored data for such processes as frame averaging. The IM-RTP contains a 15-MHz, 1000-MIPS programmable pipeline processor that lets you simultaneously perform as many as seven operations. For a 512 × 512-bit image, this translates into a processing rate of 50 frames/sec.

The IM-RTP lets you do real-time image subtraction, temporal filtering, and edge detection. The board also provides hardware support for binary, recursive, and gray-scale morphology, spatial filtering, statistics, and point-to-point transforms. This processor also lets you define a region-of-interest (ROI) and limit the processing to that region. Furthermore, statistics that you associate with object labels are performed in parallel on every object. Therefore, the time it takes to extract the statistics is independent of the number of objects in the image.

The IM-CLD color module accepts NTSC; PAL (phase alternation line), the European television broadcast standard; Super-VH; RS-170; and RS-330 video input signals. The board can digitize the red, green, and blue color components

with 8-bit or 15-bit resolution on each channel. Using this board, you can acquire and display true-color images in real time. The IM-CLD also performs full-resolution color-space conversions to and from RGB, HSI (hue, saturation, intensity), and YIQ (intensity, in-phase, quadrature-phase). This module has four analog video-input channels, so you can perform real-time switching between multiple video sources.

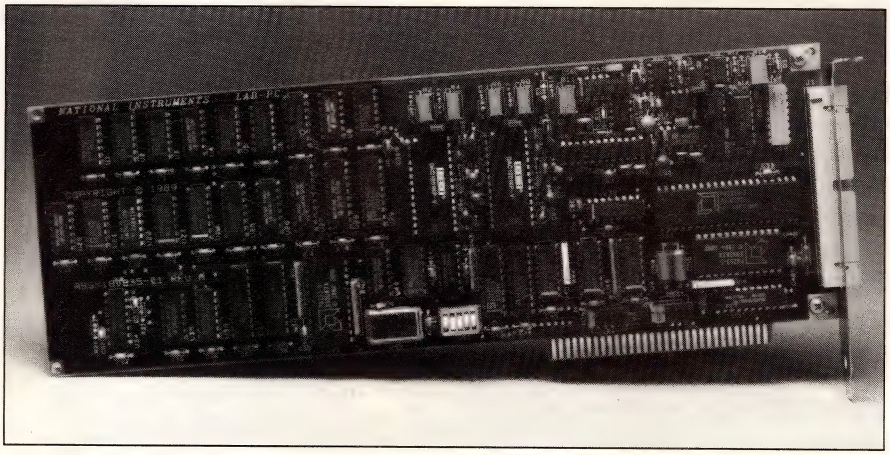
The IM-ASD asynchronous digitizer monochrome monitor can also accept video inputs from four analog sources, or from one digital source. You can feed this unit 16-bit digital signals at programmable frequencies ranging from 0 to 30 MHz. This board digitizes analog information at 8 bits/pixel with a sampling frequency reaching 15 MHz. The board can also generate synchronization signals to define both external and internal synchronization relationships.

The Image Series boards are scheduled for shipment in December 1989, except for the IM-CLD, which will ship during the first quarter of 1990. Pricing for the Image Series is expected to be $9995 for an IM-1280 with 1M byte of RAM, $3995 for the IM-RTP, $1495 for the IM-ASD, and $1495 for the IM-CLD. *—J D Mosley*

Matrox Electronic Systems Ltd, 1055 St Regis Blvd, Dorval, Quebec, Canada H9P 2T4. Phone (514) 685-2630. FAX 514-685-2853.

Circle No 734

Low-cost data-acquisition board for PCs offers 12-bit analog, digital, and timing I/O



***For only $695, the Lab-PC plug-in data-acquisition card** can provide your IBM PC or a compatible computer with 12-bit I/O resolution and digitize analog data at sample rates reaching 60 kHz.*

For just $695, you can buy a plug-in board for your IBM PC-compatible computer that digitizes data at rates reaching 60 kHz and offers 12-bit I/O resolution. Dubbed the Lab-PC, this board provides an inexpensive way to turn your computer into a platform for laboratory test, measurement, and control applications.

The Lab-PC lets your host monitor real-world processes via its eight multiplexed, single-ended, 12-bit analog-input channels. In addition to providing a 60-kHz max sustained sample rate, the board includes an input range of 0 to 10V or ±5V, and a programmable gain of 1, 2, 5, 10, 20, 50, or 100. A 16-word FIFO A/D buffer helps prevent bus latency. You can use this multichannel analog input for temperature measurement, signal analysis, data logging, chromatography, and dc voltage measurement.

The Lab-PC board also has two 12-bit, double-buffered analog-output channels that you can use to control external systems and generate stimulus waveforms for test and measurement applications. Three counter/timers with clock rates reaching 2.6 MHz measure time-critical signals to provide a means for synchronizing events, generating pulses, and measuring frequency and time.

Furthermore, Lab-PC's 24 digital I/O lines provide a path for intermachine communications, for switching external devices such as transistors and solid-state relays, for reading the status of external digital logic, and for generating interrupts. These I/O lines come configured as three 8-bit ports, software-configurable for input, output, or bidirectional transfers. Two-wire handshaking modes and interrupt generation provide additional control.

To develop application programs for the Lab-PC, you can use either the $95 Lab-PC LabDriver library of software routines or the $495 LabWindows Version 1.2 instrumentation software package.

LabDriver is an inexpensive collection of high-level software routines that simplifies application programming and reduces development time. Included among these routines is support for analog, digital, and counter I/O devices; for high-speed data acquisition; and for waveform generation. You can order Lab-PC LabDriver libraries for either Microsoft C or QuickBasic languages.

You can also use the manufacturer's LabWindows Version 1.2 instrumentation software to develop data-acquisition and data-analysis programs in Microsoft C or QuickBasic. Version 1.2's intuitive interface provides function panels for interactive configuration of the Lab-PC board. Each function panel automatically generates Microsoft C or QuickBasic source code, which you can then execute interactively or compile as a stand-alone application. Additional enhancements include strip-chart generation, improved graphics-printer support, more powerful data-formatting capabilities, and better data safeguards in the interactive environment.

LabWindows includes libraries for formatting, analyzing, graphing, and storing data. IEEE-488 and RS-232C capabilities make it easy for you to integrate stand-alone instruments in systems that already include data-acquisition boards. (The LabWindows Instrument Driver Library alone contains more than 60 ready-to-use modules for controlling IEEE-488 and RS-232C instruments.) For an additional $895, you can also order an optional Advanced Analysis Library.

—J D Mosley

National Instruments Corp, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 433-3488; in TX, (512) 794-0100. FAX 512-250-9319.

Circle No 733

Z I L O G

Z8 CCP™

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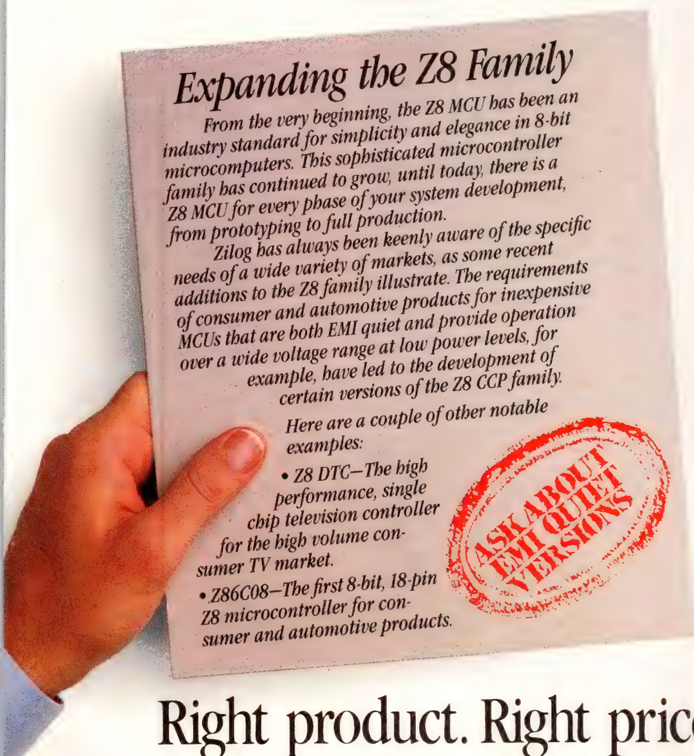
The low-cost Z8 CCP family of microcontrollers takes full advantage of Zilog's new Superintegration™ Z8® core. The result is unprecedented functionality at a price that makes sense for high volume consumer and automotive products as well as intelligent embedded peripherals.

Features . . .

For starters, there's a voltage detection circuit that automatically triggers an on-board power-on reset timer for no-fuss power up. And it continues to provide brown-out protection . . . in case Vcc falls below the 2.5-5.5 volt operating range. Not only that, there's an on-board watchdog timer that secures your application even further.



. . . and more features.

You also get a stop mode that typically consumes less than 2 microamps. What's more, stop-mode wake-up and interrupts can be triggered from multi-input port transitions, making the Z8 CCP MCU ideal for key-pad applications. And that's not all. The Z8 CCP series gives you on-board analog comparators, two 8-bit counter/timers, with 6-bit pre-scaler, and the right amount of I/O. And you know you're going to get very fast code development, because you've got full compatibility with the widely used 8-bit Z8 instruction set.

And plenty of important choices.

Choose between low EMI wide voltage range or high-speed control devices. The Z8 CCP microcontroller is also available in your choice of RC, ceramic or crystal oscillator circuits. And in 18-, 28-- and 40/44-pin versions, in a variety of packages, with 2K or 4K ROM Code sizes. All off the shelf and backed by Zilog's proven quality and reliability.

To find out more about the Z8 CCP MCU or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

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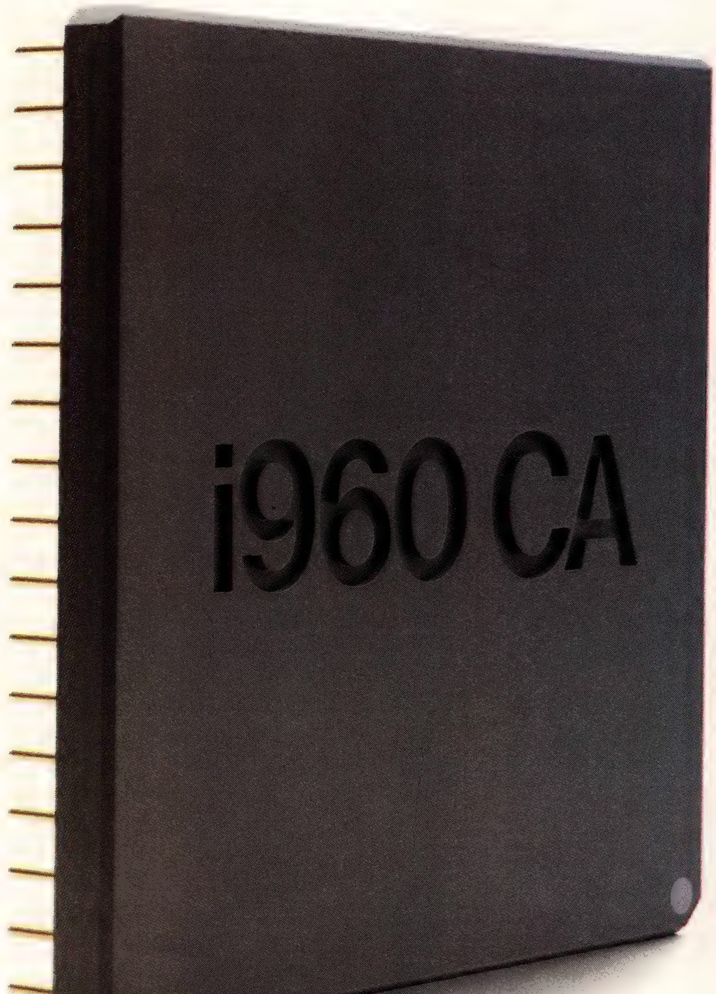
CIRCLE NO 117

Multiple instructions per clock is not a barrier.

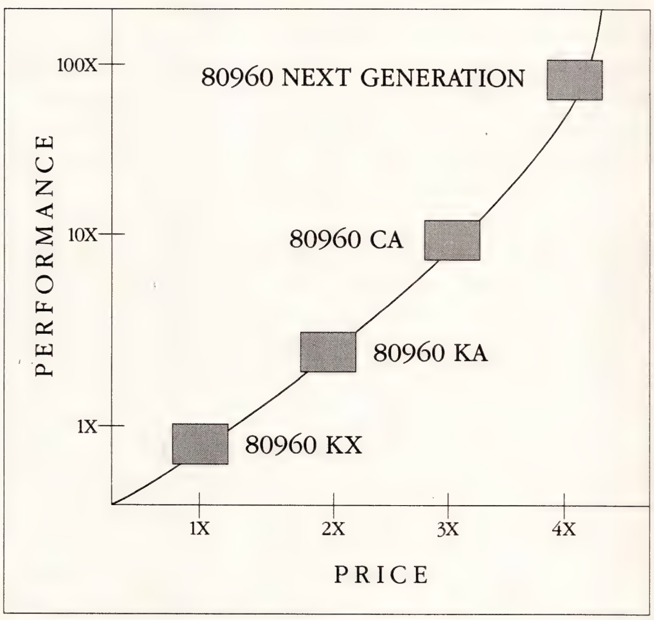


It's a milestone.

Multiple instructions per clock is now a reality. Intel's new i960 CA is the first 32-bit embedded processor to execute multiple integer and control instructions per clock.

The i960 CA is the first processor to implement SuperScalar architecture on a single chip. It consistently breaks the multiple instructions per clock barrier because it looks ahead in the data stream and selects groups of instructions to safely begin executing at the same time.

Thus the i960 CA allows you to reduce design costs by using less expensive memory and peripherals,



For 32-bit embedded control, i960 architecture offers a broad and growing range of price-performance options.

at the same time you enjoy its unprecedented performance. In its 33-MHz version, the i960 CA can sustain 66 native MIPS.

But as pleased as we are with its performance, we're also proud of the i960 CA as an Intel milestone. It's part of the i960 family of products that will remain software-compatible for generations.

The world's most highly integrated 32-bit embedded processor:

- □ Instruction cache: 1-kb, two-way, set-associative
- □ SRAM: 1.5 kb one-clock access (15 frames 16 × 32 bit registers)
- □ General purpose registers: 32 × 32 bit
- □ I/O channel processor: data chaining, 4-channel DMA's
- □ Interrupt processor: 248 possible vectors
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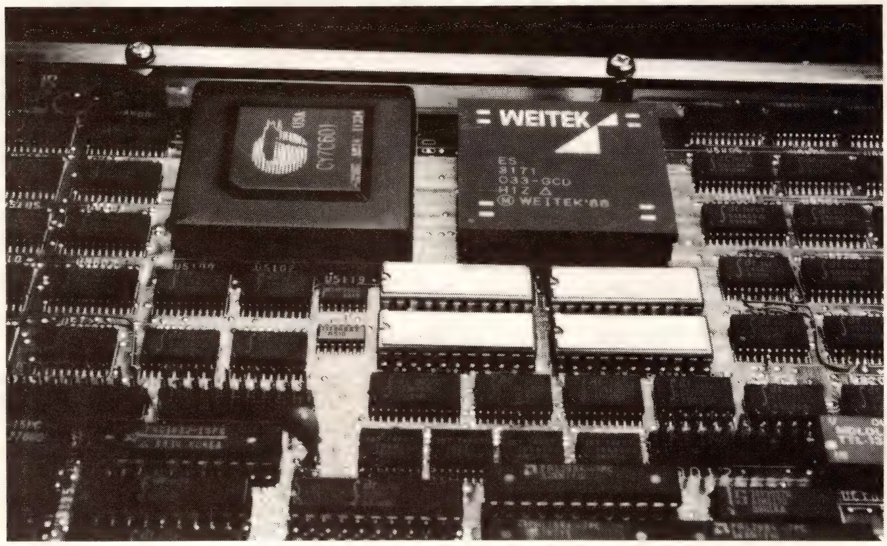
Upgrade lets workstations operate at 65 MIPS in 4-processor configuration

The Series5 is a board upgrade to the first-generation SPARC-based Series4 family of workstations. The board uses the Cypress Semiconductor (San Jose, CA) 33-MHz SPARC CPU and the Weitek (Sunnyvale, CA) 3171 floating-point processor to achieve single-processor performance of 22 MIPS and 3.0M flops. The architecture of the Series5 can accommodate as many as four processors, which increase performance to 65 MIPS and 8.9M flops.

A 128k-byte physical cache, controlled using GaAs PLDs, aids performance of the Series5. The physical cache eliminates some design inefficiencies and limits data contention, where certain memory locations are used more frequently when creating and using the address index; the cache also limits data flushing. In a multiple-processor system, each processor works with identical data addresses. The alternative, a virtual cache, sets up arbitrary addresses in the virtual cache index that wouldn't necessarily map to the same data in another processor's cache index. The GaAs cache controller compensates for the performance penalty of using a physical cache by translating logical addresses to their physical counterparts.

In addition to the 128k-byte cache memory, you can configure the workstations with error-checking and -correction RAM in 16M- and 32-byte increments and with as much as 2.6G bytes of SCSI disk storage on the workstations or 13.3G bytes of SMD (Storage Module Drive) storage on the Series5/800 SuperServer.

A proprietary 64-bit bus on the board that operates at 128M bytes/sec achieves high computational throughput. Five extra slots provide room for expansion on the Series5/530 and /800 servers and /500 workstation; the Series5/670 server and /600 workstation have seven expansion slots. The /670 and /800 servers and the /600 workstation also have seven VMEbus slots.



A purely physical cache, *a 33-MHz Cypress SPARC chip, an Abacus floating-point unit from Weitek, and some GaAs controllers help the Series5 CPU board attain more than 22 MIPS.*

The workstations are all binary compatible with Sun Microsystem's (Mountain View, CA) workstations—to date, the vendor has verified that more than 270 Sun applications from 125 vendors, including Sun's own diagnostics, run without recompilation. Software included with the Series5 includes the vendor's Unix-based OS/MP, a SunOS derivitive; a C language compiler; and for the user interface, SunView, the X Window System, and the X Window Manager.

The machines are protected with a 12-month service and support warranty. The vendor assumes responsibility for slot management of your machines; for example, if you buy 32M bytes of memory on two 16M-byte cards and you need a slot later, the vendor will reconfigure the system with a 32M-byte card. You don't pay for memory-board swap—just the cost of the new application board.

Typical server pricing ranges from $33,400 for a Series5/531 with one processor, 16M bytes of RAM, a 327M-byte disk, and 150M bytes of SCSI tape storage to $172,600 for the /800 with four processors, 64M bytes of RAM, 3.3G bytes of SMD storage, and 2G bytes of Exabyte storage. Similarly, workstations can cost $28,900 for a diskless, uniprocessor, desktop Series5/501 with 16M bytes of memory. The /604 deskside workstation with four processors, 64M bytes of RAM, and 661M bytes of disk storage costs $122,400.

—Michael C Markowitz

Solbourne Computer Inc, 2190 Miller Dr, Longmont, CO 80501. Phone (303) 772-3400. FAX 303-772-3646.

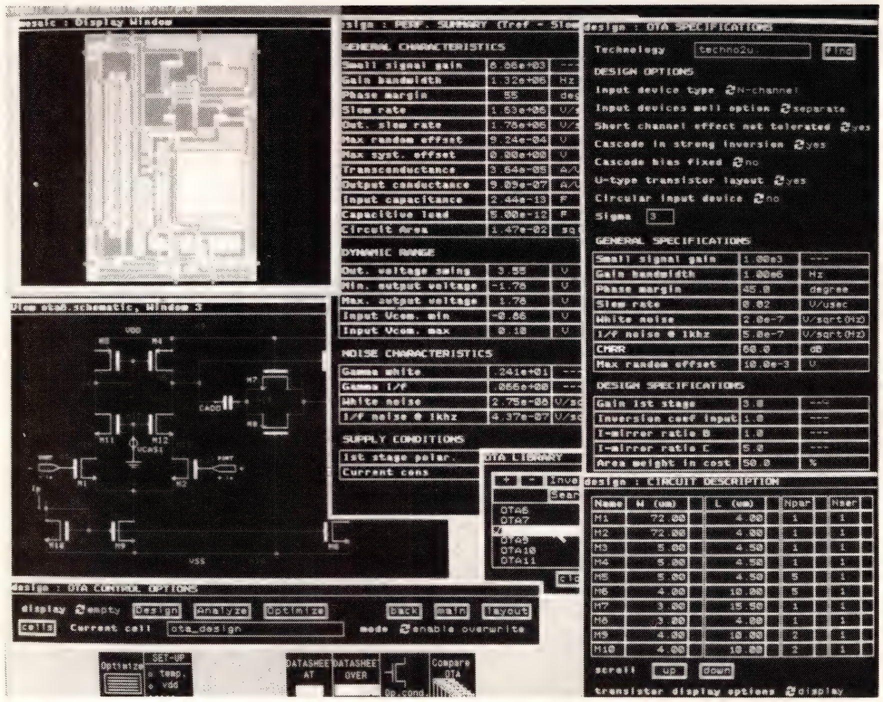
Circle No 735

CAD tools synthesize filters and generate linear blocks and circuits

Digital designers have had the ability to synthesize digital logic for a few years. Now, with Autofilter and Autolinear, analog-IC and mixed-signal-IC designers can tweak parameters to synthesize high-performance analog circuits. Each product incorporates design, optimization, and analysis facilities and is tailored to a specific type of design.

For analog switched-capacitor filter design, Autofilter uses a graphical-performance-capture capability along with its synthesis algorithms and layout techniques to combine process parameters and design objectives into a practical IC or building block. The software can have a library of pre-existing analog modules, or it can synthesize the components as the software needs them. Using a response specification as your starting point, you can compress the time required to design and layout a filter from one month to a day, according to the vendor.

Within Autofilter, you can modify key variables, specify acceptable performance ranges, select tradeoff paths, or accept the software's parameter defaults. Filter synthesis lets you choose a symmetrical bandpass/bandstop or a nonsymmetrical bandpass filter. You can adjust cutoff frequencies, ripple, gain, rejection, sample frequency, and filter approximation type (elliptic, Butterworth, Chebyshev, or inverse Chebyshev). The software synthesizes the z-transform and calculates the filter degree. You then can evaluate your design for filter magnitude, gain, phase, group delay, loss as a function of frequency, and the filter's poles and zeros in the complex plane. Better, you can graphically interact with the poles and zeros to add, move, or delete them to tailor the circuit's response.



A unified design, optimization, and analysis tool *for creating analog building blocks, Explorer Autolinear takes high-level input specifications and produces a process-specific layout.*

Autofilter also synthesizes switched-capacitor filters based on cascaded biquad topologies. Further, the software provides a user-specified cost function between noise sensitivity and capacitor area to let you make important design decisions. For the balance of the design process, Autofilter provides data output in standard formats, such as GDSII, Spice, and Switcap, as well as in the vendor's GDT Designer format.

Autolinear, which works from a high-level specification, is a synthesis and module-generation tool for creating analog building blocks. In addition to addressing process, voltage, and temperature effects on the circuit, the software also understands and considers transistor matching and noise coupling when it synthesizes the layout. An analysis mode lets you see how close the software came to meeting your specification and helps you decide how best to proceed with the design. If the software can't meet your performance goals using the physical topology you chose, it suggests ways to modify the design. Finally, you can optimize the circuit for such analog parameters as current consumption and area.

Autolinear contains a host of analog building blocks, such as operational transconductance amplifiers, op amps, comparators, voltage references, current references, resistors, capacitors, transistors, and crystal oscillators. The software speeds the synthesis and analysis

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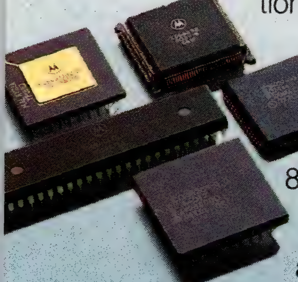

The most recent additions to the 1230's long list of supported micros include Intel's 80286 and 8096 and Motorola's 68332, 68010 and 68HC11.

Bus analysis is also part of the 1230's exceptional support package.

Installation of probes and personality modules is effortless; the disassembly itself is more complete and informative than anything else in its class. You can have a complete 8-bit microprocessor debug package, including logic analyzer, for under $4000, and a 16-bit package for under $6000.

Start with 16 channels. Expand in 16-channel increments to a maximum of 64. On-screen help notes, pop-up menus and automatic prompts make the 1230 exceptionally easy to learn and use. Yet you can access features like four 2K deep memories, sophisticated triggering and built-in babysitting mode that are unprecedented in this price range.

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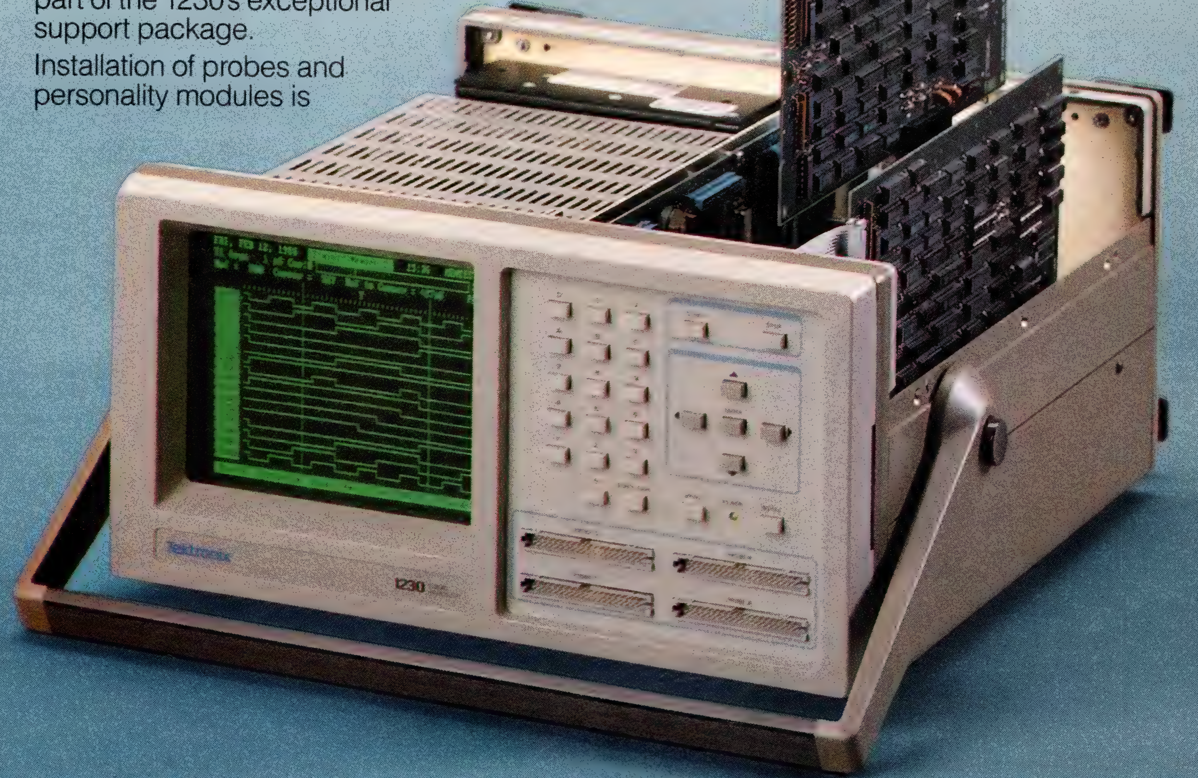

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of your circuit and circuit elements, yet it gives you enough control to manually optimize the design. Autolinear yields output in the Graphics Design System II (GDSII) or Cal-Tech Intermediate Form (CIF) layout database, in a Spice net list, or in the company's L(r) layout database.

Both software packages fit into the vendor's Foundation design framework. The tools are part of the modular Explorer series of IC design software, which you can purchase in stand-alone or mix-and-match configurations. Autofilter and AutoLinear start at $40,000 on either the Sun-3 or Apollo DN4500 workstations.

—Michael C Markowitz

Silicon Compiler Systems, 2045 Hamilton Ave, San Jose, CA. Phone (408) 371-2900.

Circle No 732

WHAT'S NEXT IN EDN

EDN Magazine's November 9, 1989, issue will provide advanced information on Wescon/89—what you can expect at the technical sessions and what new products will be displayed at the show. Our Special Report will cover low-cost workstations—those machines that range in price from $4000 to $20,000. Other scheduled articles include

- An update on surface-mount technology
- Part 2 of American engineers in Japan
- Coverage of object-oriented programming

. . . and much more. And in our next issue, look for EDN's 16th annual microprocessor directory.

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CIRCLE NO 44

Graphics environments

A standard graphics environment for open systems would enable software vendors to develop application code that is portable across heterogeneous systems, such as those made up of computers with different μP families, bus structures, or operating systems. Many believe that evolving standards will meet portability goals and provide a common look and feel across applications.

Maury Wright, *Regional Editor*

EDN SPECIAL REPORT

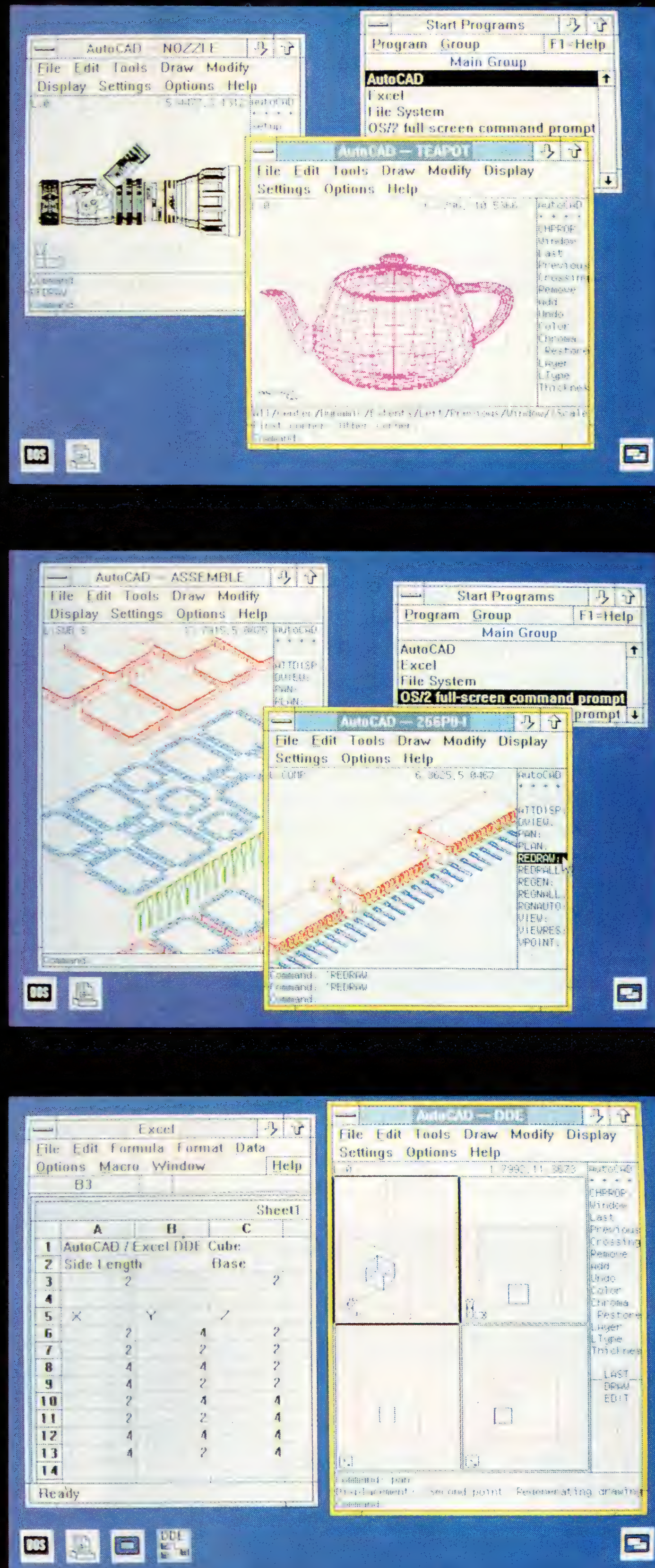
Neither software vendors, data-processing managers, nor end users can or want to live with different versions of software for every different system. The logistic and technical challenges posed to the software vendor drive up the price of software and ensure that products will only be available on selected popular systems. And end users demand better software at lower prices. A single standard graphics environment could solve the problem. A standard might enable software vendors to offer highly functional low-cost software, such as that available for the multitude of X86-based systems, for heterogeneous systems. Such a set of systems could include IBM PCs, Sun workstations, and DEC minicomputers. And custom software developers could write equally portable code.

Consider Autodesk, the manufacturer of the best-selling CAD software AutoCAD. The company offers its software in nine versions: Ultrix and VMS versions for DEC systems; a SunView version for Sun workstations; an Apollo version; an Apple Macintosh version; and MS-DOS, extended MS-DOS, OS/2 PM, and Xenix versions for X86-based systems. The logistics of supporting so many different versions of the same software equal the technical challenges of porting AutoCAD to new hardware-software combinations. Simple incremental releases for bug fixes or added functions propagate across the entire product line. Furthermore, within a single product such as the MS-DOS version, Autodesk must provide operating system drivers for all the popular standard graphics boards (CGA, EGA, VGA, Hercules, and selected high-performance nonstandard boards) and plotters and printers.

Graphics standards are the key to any hope of application software portability in a heterogeneous world of computing or even device independence among homogeneous systems, such as Macintosh computer systems. In general, computer manufacturers, software vendors, and users now endorse the idea of standard open systems including graphics environments and associated GUIs (graphical user interfaces) that make using the

environments and application programs simple. Microsoft Windows for MS-DOS and Presentation Manager for OS/2 have emerged as standards for the wide variety of systems based on Intel X86 μPs. A universal graphics-environment standard should embrace all systems, but especially Unix. Although the heterogeneous software and system industry endorses standard open systems as a concept, the same industry can't yet agree on a single standard graphics environment and underlying operating system.

Choosing a graphics environment as an end user or as a system designer or integrator is a risky business. Currently, no single standard graphics environment exists, and, therefore, not all application software may run in the environment you choose. Independent software vendors would like to support a single graphics environment with graphics-based application software. Furthermore, the vendors would like the graphics environment and application to be hardware independent. Of potentially greater importance, the internal data-processing departments in com-



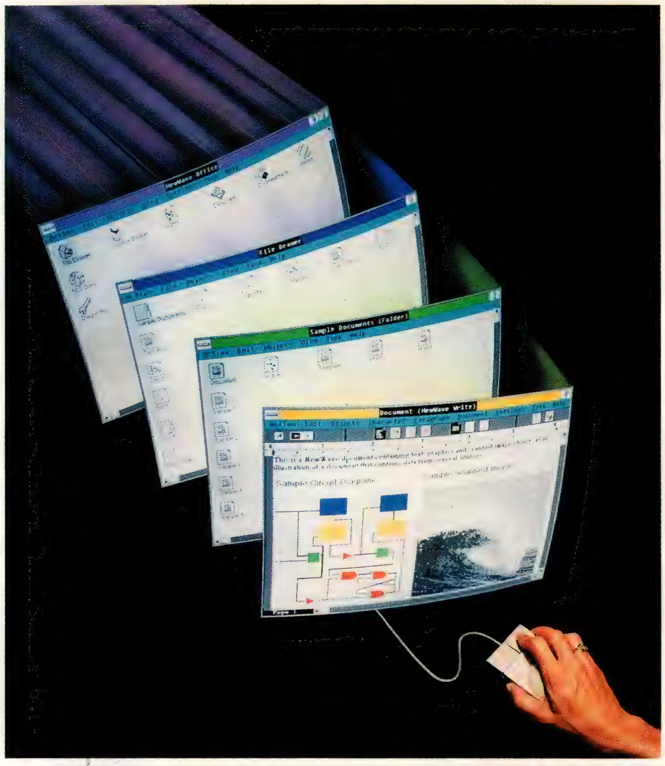
You can choose from a number of popular application packages for Presentation Manager, and the graphics environment provides communication links to let applications work together simultaneously. (Photo courtesy Microsoft Corp)

Windows for MS-DOS and Presentation Manager for OS/2 have emerged as de facto standards that result in device independence for X86-based systems.

panies need to support custom software on a wide variety of hardware and operating systems. And increasingly, companies don't exclusively buy from a single closed-system vendor such as Digital Equipment Corp (DEC) or IBM.

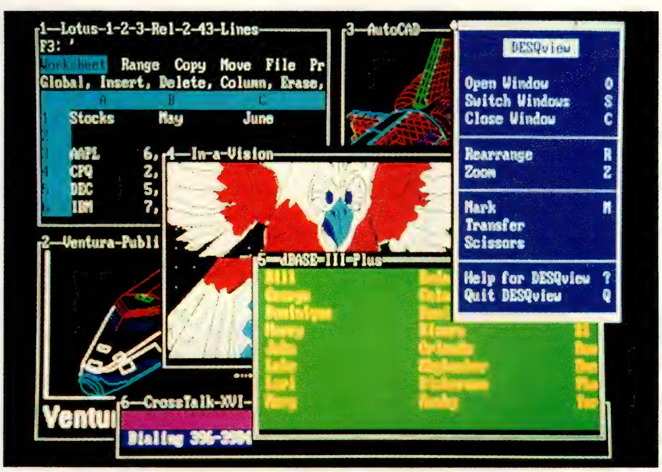
A number of different partitions, or modules, comprise a graphics environment. A GUI is only a specification of how application programs look and feel, or appear and behave, to the user. Graphics environments typically have libraries or tool kits that let application programmers implement the GUI look and feel by using traditional development tools, such as compilers. An operating system and the underlying hardware form the basis of a graphics environment. Other features of a graphics environment, such as desktop managers, file managers, and window managers, are typically application programs that are closely coupled with the GUI and operating system.

Computer users like, want, and even need GUIs—the Apple Macintosh is proof. The look and feel common to applications based on a GUI let users learn and use new application software quickly. Furthermore, typical window-based GUIs and their underlying graphics environments provide a logical and understandable multitasking metaphor that mimics a desktop work environment.



The object-oriented user interface and persistent-link capability in Hewlett-Packard's NewWave demonstrate the future of graphics environments.

Only a handful of graphics environments exist for open systems, although virtually every manufacturer of closed systems has some proprietary form of a graphics environment. DESQview from Quarterdeck, GEM (Graphic Environmental Manager) from Digital Research, and Windows from Microsoft all run in conjunction with MS-DOS on systems based on Intel X86 μPs. The DESQview program is actually character based but can manage graphics-based applications. The OS/2 PM (Presentation Manager) combination from Microsoft also runs on X86-based systems.



Standard MS-DOS programs as well as Windows and GEM applications can run under the control of Quarterdeck's DESQview in a multitasking environment.

For heterogeneous systems, you can choose between Motif from the Open Software Foundation (OSF) or Open Look, which is endorsed by the Unix International consortium and sold by AT&T. The NextStep graphics environment from Next Inc (Palo Alto, CA) has also been licensed to IBM, and Next may choose to offer licenses to other system manufacturers. Microsoft may also offer a version of Presentation Manager for Unix systems.

Graphics environments don't match a model

Comparing graphics environments is quite confusing. No equivalent to the networking 7-layer Open System Interconnection model exists for graphics environments, and comparing two graphics environments is not necessarily the apples-and-apples comparison some people make it out to be. Not all graphics environments have a defined imaging model—a library of software

routines that implement basic graphics functions—and windowing functions can be implemented in different ways in different environments. Some graphics environments are integrated inseparably with operating systems; others you simply add to an existing operating system. All graphics environments do have some form of an application program interface (API) that application programs make calls to. A call directly from an application program to an operating system, for example, to get a character from the keyboard, is the simplest example of an API. The tool kits and libraries mentioned earlier implement higher-level graphics APIs.

The API calls act as middlemen and provide the means by which you can develop system-, CPU-, and device-independent source-level application software. **Fig 1** shows a block diagram of the MS-DOS/Windows environment and provides a visual aid to understanding a typical graphics environment. You can see that the MS-DOS/Windows environment supports API calls at two different levels. MS-DOS includes a basic set of API calls, commonly referred to as the BIOS, for character- or text-based application programs. Most existing MS-DOS application programs employ a combination of calls to the BIOS and code that interacts directly with specific hardware.

Windows applications can only use the set of API calls implemented in the graphics device interface (GDI). Some GDI calls, such as reading a block of data from a disk, map directly to MS-DOS BIOS calls. Other API calls implement the graphics functions supported by Windows. Because Windows applications use only API calls, the applications no longer communicate directly with hardware and in particular with graphics hardware. Therefore, Windows applications are device independent. A graphics-board manufacturer simply provides a Windows-compatible software driver along with a graphics board. Windows users can therefore choose graphics displays and plotters and printers that best meet their needs rather than choosing devices supported by a specific software package.

Windows provides users of X86-based MS-DOS computers with a full-function graphics environment and a list of available application software that seems to grow daily (see **box,** "Windows for engineers now, PM later"). Windows took a long time to catch on because Microsoft shipped the product late and early versions had many bugs. Most software developers claim that the product has now been stable and well behaved for 18 months or more. You can expect a number of major vendors such as Wordperfect (Orem, UT) and Ashton-Tate (Torrance, CA) to announce Windows products late this year. Windows costs $99 for the 80286 version and $195 for the 80386 version. You can also expect a new release of Windows in the next six months that improves memory-management and multitasking features and offers an improved 3-D appearance.

DESQview and GEM also serve certain niches in the MS-DOS market. Quarterdeck's DESQview runs virtually all MS-DOS software in a windowed multitasking environment. According to Quarterdeck president and cofounder Therese Myers, the company realized from the start that no software vendor would develop specialized code for a graphics environment offered by a start-up company. Quarterdeck developed a way to intercept BIOS calls and calls made directly to hardware; therefore, DESQview can run MS-DOS software unmodified. In fact, DESQview will run on the entire range of MS-DOS machines ranging from 8088-based systems to the newly announced 80486-based systems. You can even run Windows and a Windows application in a DESQview window.

Quarterdeck has also started promoting a set of DESQview API calls and encouraging DESQview-spe-

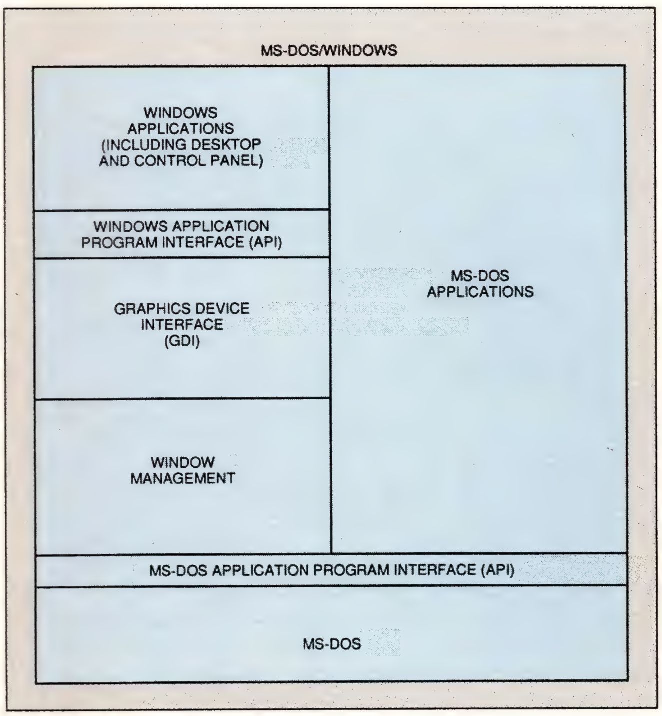


Fig 1—API calls to the graphics device interface let Windows applications function independent of the specific graphics hardware present in a system.

Graphics environments offer users the first tremendous increase in functions and, therefore, work efficiency since 64k bytes of memory were dedicated to CP/M users.

cific application developments. Most of the developer interest is for custom applications rather than commercial packages. For example, Quarterdeck offers an API library for DBase III software development. DESQview, however, will remain a viable operating environment for some time to come because of the reluctance of many users to buy new hardware or software. The standard version of DESQview sells for $130; a 80386-specific version costs $190.

Digital Research developed GEM for the development and support of its own suite of graphics application programs, such as GEM Draw and GEM Desktop Publisher. The company also chose to offer GEM as a graphics environment to other graphics software developers. A number of well-known applications such as Ventura Publisher are based on GEM. A stand-alone version of GEM costs $50.

Digital Research recently began promoting GEM as a tool that can act as a bridge between different heterogeneous operating environments. GEM does not include the complexities that Windows does to handle features such as multitasking; GEM simply serves as a graphics tool kit on which developers can base applications. Digital Research has ported the GEM graphics environment to other systems, such as Atari personal computers and its own FlexOS real-time operating system, and has started calling it X/GEM (Extended GEM). The company also plans to offer an OS/2 PM version of X/GEM.

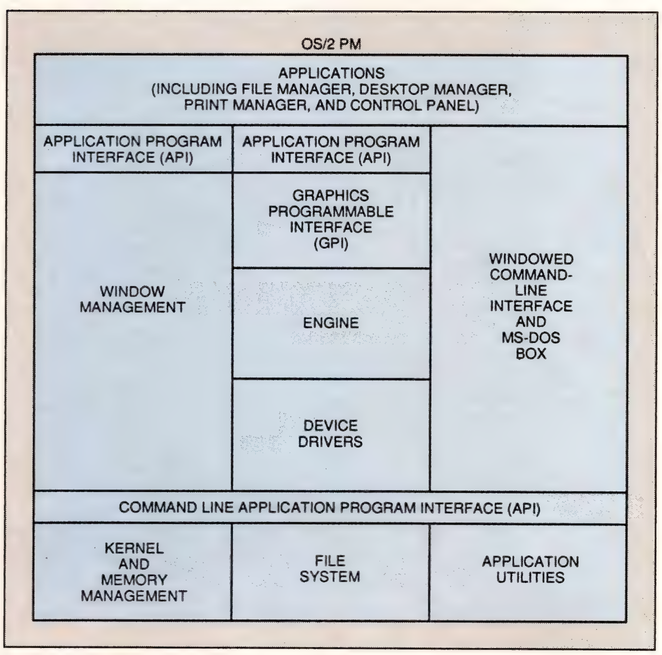


Fig 2—The graphics programming interface in Presentation Manager implements a robust set of graphics primitives that makes developing graphics applications easier than similar developments for Windows.

X/GEM project manager Bill Fitler explains that the simplicity of GEM will enable software developers to create graphics applications that can work with any X/GEM system. And X/GEM applications can run on low-end machines, unlike applications based on other graphics environments for heterogeneous systems. The port of X/GEM to FlexOS targets a different class of users—designers of real-time embedded-control systems. In fact, both DESQview and X/GEM include features that address the real-time market.

These graphics environments for MS-DOS were really afterthoughts. Microsoft designed OS/2 and Presentation Manager (PM) together as a closely coupled graphics environment. OS/2 PM provides a perfect example of a full-featured graphics environment; **Fig 2** shows its organization. OS/2 PM includes the Graphic Programming Interface (GPI), which provides a set of graphics primitive functions far exceeding the capability of Windows' GDI. The window manager implements the intuitive look and feel of OS/2 PM. And the environment includes a full set of utility application programs. Microsoft also plans to implement a printer control language for OS/2 PM that will let users match screen and printer fonts exactly.

Presentation Manager promises to bring a new level of productivity to users of X86-based systems. You'll hear pro and con arguments about the future of OS/2 PM centered around technical, cost, marketing, and application-software issues. Careful consideration, however, shows that OS/2 PM will be an unqualified success.

First, OS/2 PM eliminates the 1M-byte memory map that stifles performance in any system based on the 80286 or more powerful µPs. The graphics environment implements true multitasking and includes a facility called DDE (Dynamic Data Exchange), which handles interprocess communications. Today, Microsoft and Autodesk have a demo of Excel and AutoCAD working together using DDE under OS/2 PM. Changes in the Excel spreadsheet cause AutoCAD to redraw an image to a new specification calculated by Excel. Furthermore, you can expect a full complement of other application software for the environment to be available around the first of the year.

Critics claim OS/2 PM is late. True. Microsoft undertook a tremendous development effort to do OS/2 PM right. And application software developers had to wait

for the environment to stabilize before committing resources to a development effort. According to developers, the result is worth the wait.

Autodesk product manager John Forbes claims OS/2 PM technically equals or betters any operating system and graphics environment on the market. Forbes points out that Unix supports multitasking but that OS/2 PM supports multithreading within each task. Forbes also points out that OS/2 PM has a file system superior to that of Unix and a better defined interprocess communication capability. And remember, Autodesk offers its products for several Unix-based systems.

Glenn Goodrich, development manager at Aldus (Se-

Windows for engineers now, PM later

The growing popularity of Microsoft Windows can benefit engineers who use personal computers in the same way that it benefits office workers. Windows provides users with limited multitasking capabilities and a graphics environment in which to work. A number of useful applications for Windows exist, and more are introduced every day. And graphics-based applications typically include more or easier to use functions than text-based packages do.

To date, no CAE tools such as schematic capture exist for Windows. The leading personal-computer-based CAE software vendors all developed custom graphics environments before Windows became an accepted standard. Foresight Research (Kansas City, MO), however, offers its Drafix mechanical CAD package for Windows, and National Instruments (Austin, TX) offers its instrumentation control LabWindows package for Windows. You can also choose from a number of good drawing and graphics packages for Windows, such as Designer from Micrografx (Richardson, TX).

Most engineers also need a solid set of general business applications, and you'll be hard pressed to find better ones than some of the Windows products. For example, the Ami word processor from Samna (Atlanta, GA) includes many features associated with desktop publishers but is also fine for writing simple memos. The new Professional version of Ami includes a drawing capability, which is handy for technical documents, and a table generator. The software is worth the asking price just for the table-generation capability in technical documents.

For more complex publishing needs, Aldus (Seattle, WA) Pagemaker is Windows based and one of the two best-known desktop publishing packages. The Microsoft Excel spreadsheet offers substantially more features and has a much friendlier user interface than does the Lotus package most people are using. The DynaComm package from Future Soft (Houston, TX) implements a rich set of communication features.

Formmaker's (Mobile, AL) Horizon software lets you create, print, and fill out custom forms.

Two must-have packages are Hewlett-Packard's NewWave and PackRat from Polaris (Escondido, CA). NewWave implements an object-oriented user interface on top of Windows. PackRat includes a free-form personal information manager, a dialer, a note-taking capability, and other features. In short, use PackRat for anything that doesn't fit neatly into more conventional software packages.

Expect OS/2 and Presentation Manager to entice you soon as well. All of the Windows packages mentioned will be available for OS/2 around the end of the year. In addition, Borland's (Scotts Valley, CA) Sidekick for OS/2 is super, and you can expect an OS/2 version of AutoCAD from Autodesk (Sausilito, CA) by the time this article appears. In 1990, expect one or more of the major personal-computer-based CAE vendors to port to OS/2 as well.

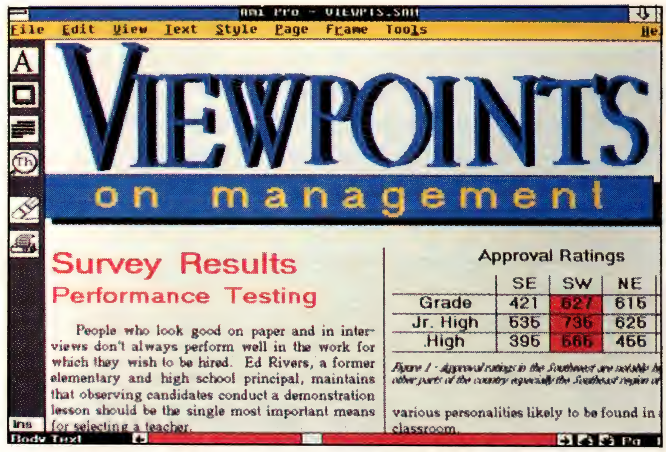
For custom software development for Windows and Presentation Manager, Caseworks (Atlanta, GA) offers tools for both environments that make creating the user interface painless. Currently, the company only offers products for C-language developments, but Fortran and Cobol products are also planned. Graphic Software Systems (Beaverton, OR) offers its XVT (Extensible Virtual Toolkit) that lets you develop code that is portable across the Macintosh, Windows, Presentation Manager, and X Windows graphics environments.

A graphics environment typically includes a graphical user interface, a graphics library or tool kit, and the underlying operating system and hardware.

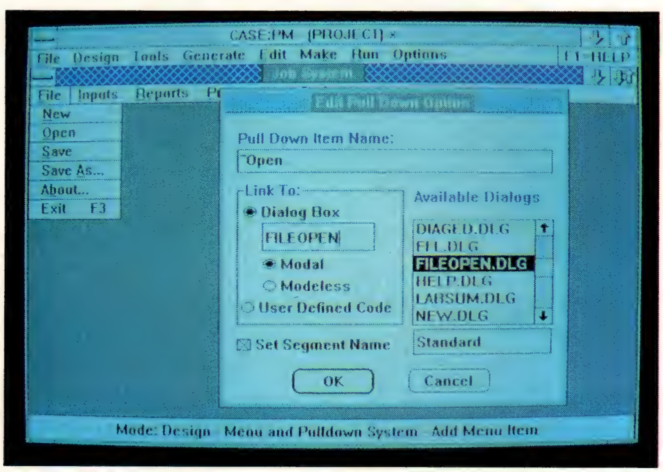
attle, WA), is also impressed with the capabilities of OS/2 PM. Aldus plans to ship Pagemaker for OS/2 PM by the time this article appears. Goodrich is especially interested in the DDE capabilities of OS/2 PM. He points out that Pagemaker is an integrating type of software package and constantly depends on communication links with other software products.

OS/2 PM achieves efficiencies compared to Unix because OS/2 PM is an environment for a homogeneous class of systems. For example, OS/2 PM only supports its own native network capability. Furthermore, the environment is tuned for a particular hardware architecture. The graphics API matches exactly the needs of PM rather than implementing a general set of graphics functions. Version 1.1 is usable and stable; version 1.2, which is due late this year, features a better desktop manager, 3-D appearance, and better performance.

Despite its technical merits, people may still have reservations about OS/2 PM. It won't run on 8088-based machines, and users will not simply throw out those old machines. In fact, many users don't need OS/2 PM and will remain perfectly happy with MS-DOS-based applications. You can, however, be misled by the prices bantered about in the trade press for OS/2-PM-based hardware and application software. The graphics environment itself retails for $350 compared with about $150 to $250 for MS-DOS plus Windows. Application-software vendors, however, don't plan to charge large premiums for OS/2-PM software. Autodesk charges $3000 for any version of AutoCAD. Aldus plans to charge about $100 more for OS/2 PM Pagemaker than it does for MS-DOS/Windows Pagemaker. This increase, however, reflects new features, not a surcharge based on the operating environment.



The table-generation facility in Samna's Ami word processor for Windows can size tables dynamically and continue them from one page to the next.



Generating dialog boxes and menus for Presentation Manager is trivial when you use the Case tools offered by Caseworks. The company also offers a similar set of tools for Windows.

Consider hardware costs also. Some OS/2-PM critics claim that a suitable complement of hardware for the environment is overly expensive. Actually, the type of user that is a likely candidate for OS/2 PM needs an equally expensive machine to attempt to accomplish a similar class of tasks with MS-DOS and Windows or DESQview. The key hardware requirements for OS/2 PM include a minimum of 3M to 4M bytes of memory and a moderately fast disk drive—the type typically shipped with 80286- and 80386-based systems.

Don't immediately assume that you need a 33-MHz 80386 to run OS/2 PM. A number of other factors, such as memory configuration and the graphics controller, can matter more to performance than the CPU type or speed. In fact, OS/2 PM and MS-DOS/Windows share the problem of added overhead due to application code that communicates with hardware via an intermediate graphics standard rather than directly. All software and systems based on graphics standards share this problem. Luckily, the fast CPUs and coprocessors currently available make the effect of the overhead negligible.

An intelligent graphics controller, such as the NEC (Wood Dale, IL) Multisync Graphics Engine based on the 34010 graphics coprocessor, makes even slow 80286-based systems run OS/2-PM applications with more than acceptable speed. Graphic Software Systems (Beaverton, OR) designed the board and offers it on an OEM basis; NEC sells the product through retail channels. The board retails for $1495 to $1995 based on configuration, but you can expect the price of copro-

cessor-based boards to steadily drop in the next year.

You might argue that, logistically, a graphics environment based on Unix might better serve users of X86-based computers than will OS/2 PM. All aspects of the computer industry will benefit from a standard open graphics environment for heterogeneous systems. Unfortunately, a single accepted Unix-based standard is at least a year away and probably more. Until such standardization occurs, most independent software vendors will maintain a wait-and-see attitude.

Users needed OS/2 PM capabilities last year and will at least realize them this year. Furthermore, because of its size, the X86-based market can support and in fact thrive with its own standard graphics environment. The potentially large sales entice application developers to port existing software to OS/2 PM and create new applications that take advantage of the features of OS/2. Basing software on MS-DOS/Windows and OS/2 PM for X86-based systems will also enable software and hardware vendors to offer standard bridge products to Unix-based systems.

Standard environment to be Unix based

A Unix-based graphics-environment standard will play a key role for X86-based systems in the future, however, and an even bigger role for the heterogeneous computing industry. Virtually every computer and software vendor in the free world is involved in one or more efforts to develop standard open systems.

Standardization efforts primarily revolve around three industry trade associations and, in general, around the Unix operating system. The first trade group, X/Open, was formed in 1984 as a nonprofit consortium of computer systems vendors. X/Open's goal was to define a common applications environment that would include a set of integrated industry standards for the development and use of applications across all compliant systems.

X/Open publishes the "X/Open Portability Guide," which contains a portfolio of API standards that ensure the portability of code at the source-code level. You can purchase the guide for $130 from Prentice-Hall (Englewood, NJ). The X/Open guidelines, however, don't specify implementation details or define a specific graphics tool kit or GUI.

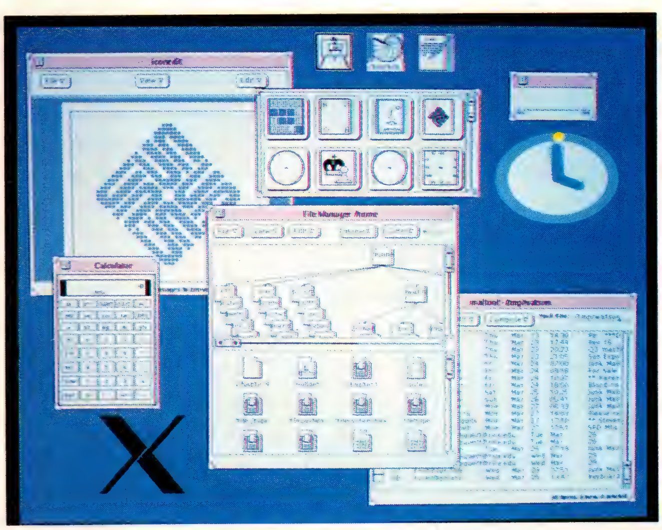
Unix International and the Open Software Foundation (OSF), both active members of X/Open, have taken the standardization effort a few steps further. The efforts of both organizations have targeted the definition and development of a standard graphics environment including a standard version of Unix, the X Windows basic graphics standard, a standard graphics tool kit, and a standard GUI.

The two organizations originated from a single industry group called the Hamilton Group, which was formed to discuss and negotiate future Unix features with AT&T. About two years ago, however, Sun and AT&T agreed to merge Berkeley and System V Unix and create a single Unix standard. Some members of the Hamilton Group and some members of the computer industry at large feared that the Sun-AT&T alliance would give the two companies a competitive advantage relative to new versions of the Unix operating system.

OSF to support itself as software vendor

A group of vendors led by IBM, DEC, and Hewlett-Packard split from the Hamilton Group in May 1988, and formed the Open Software Foundation—a not-for-profit corporation that acts as a neutral supplier of open-software technologies. The OSF is staffed and funded by sponsoring members, but within a few years it will be self-sufficient. The OSF chose to use IBM's AIX version of Unix as a base. This operating system is called OSF/1 and will feature a streamlined, modular, re-engineered kernel.

The OSF operates via a process that it calls RFT (Request For Technology). For example, the OSF issued an RFT for a GUI for OSF/1 in July 1988. A total of 39 companies submitted ideas based on the RFT. The OSF chose the best of the ideas and used them



Open Look applications available for Sun workstations include the standard desktop manager and SunPaint, SunDraw, and SunWrite.

Application program interfaces (APIs) provide the means by which graphics environments offer hardware independence.

to define the GUI called Motif. Motif is primarily based on OS/2 PM behavior, has a 3-D appearance developed by Hewlett-Packard, and employs a DEC tool kit of widgets, such as dialog boxes, scroll bars, and buttons.

Trade group acts as go-between

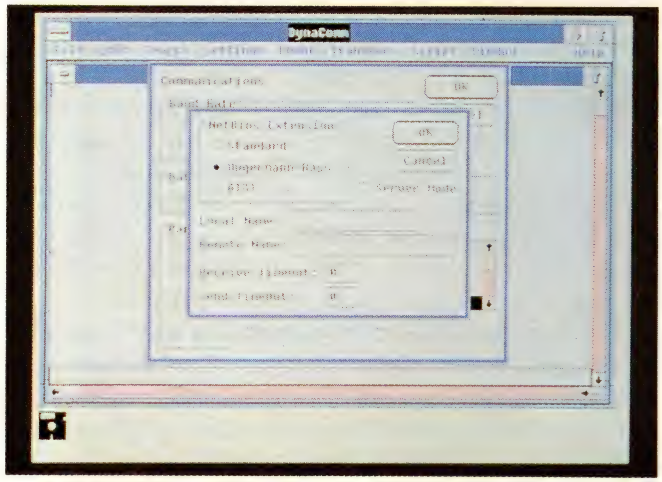
The companies remaining in the Hamilton Group, led by Sun and AT&T, formed Unix International. Unix International operates as an industry trade association and has close ties to AT&T's Unix Software Operation (USO). Unix International doesn't develop or sell software but rather helps AT&T's USO plan the development road map for future Unix versions based on input from its members. Unix International members also get early glimpses of source code and a voice in distribution and licensing issues. Membership fees can range from $10,000 to $500,000 per year based on the size of your company and the class of membership you buy.

Unix International settled on a GUI called Open Look that was developed by Sun for AT&T. The standard Open Look graphics environment will be based on the upcoming release 4 of Unix System V by AT&T's USO. Thus far, the products defined by the OSF and the products developed by AT&T's USO in conjunction with Unix International all comply with the X/Open guidelines. Open Look and Motif have comparable features but are far from compatible.

Both share a common building block, however—X Windows, a software standard that implements graphics primitives, such as drawing a circle. The Open Look products offered by AT&T's USO and the OSF's Motif products all use X Windows as the basic graphics standard. Code for X Windows is very complex and often inefficient, but X Windows has emerged as a graphics standard and has been ported to a variety of computers. X Windows also includes a network client/server model that lets graphics applications run one place on a network and be displayed elsewhere.

X Windows keys standard

Engineers at the Massachusetts Institute of Technology developed X Windows, and you can buy the latest version, X11, for $400 from the MIT Software Center. Most system vendors now offer X Windows as a system tool. Other independent companies, such as Integrated Computer Solutions, offer X Windows support, training, and versions of X Windows for some systems. Integrated Computer Solutions also serves as the corporate sponsor for the X Windows User Group.



The first communication package for Windows, DynaComm from Futuresoft, supports both asynchronous and synchronous modes of operation.

You can buy Motif or Open Look for a number of computer systems, although application programs for them are scarce. AT&T's USO is shipping an 80386 version of Open Look for System V release 3.2 in binary form for $495 and a corresponding X Tool Kit for $695. Together, the products sell for $995. Source code for each of the products costs $17,000. Late this year, the company plans to ship release 4.0 with Open Look as an extension. The Open Look package includes window, file, and desktop managers.

Sun ships Open Look for its line of workstation products. The GUI costs $295 as an add-on to its operating system. Sun calls its graphics environment OpenWindows. It includes an X Tool kit called XView and a graphics library package that combines X11 with Sun's postscript-like News graphics library. Sun also offers three Open Look-based applications including SunWrite ($695), SunDraw ($495), and SunPaint ($495).

Motif ships and gains support

At this point, Motif seems to have more supporters than does Open Look. The OSF recently began shipping Motif. Motif includes four key components:

- a User Interface Toolkit, which includes more than 30 widgets
- a Presentation Description Language, which lets a developer use text files to describe the properties of interface components
- a Window Manager, which enforces appearance and behavior
- a Style Guide, which is a written document that specifies the flexibility and constraints of behavior.

AT YOUR COMMAND.

Motif seems to be gaining momentum as more software vendors ship versions of the GUI and more system vendors adopt it.

All components of Motif are based on X11. OSF sells a source-code license for $1000 per unit; binary licenses range from $10 to $40, depending on volume.

The Santa Cruz Operation (SCO) offers an operating system package bundled with Motif for 80386-based systems. The Open Desktop package costs $995 and includes Motif, SCO's Xsight X Windows package, a database-management package, TCP/IP (Transmission Control Protocol/Internet Protocol) and NFS (Network File System) network support, the Unix operating system, and an MS-DOS compatibility utility.

Integrated Computer Solutions offers Motif for Sun, DEC, Sony, and Apple systems. For your first CPU, the company charges only $500 for the package. This price includes the full Motif package, and the company offers support training, updates, and consulting.

Of potentially greater importance than Motif's availability as a stand-alone software product is the fact that system vendors plan to start bundling Motif with their operating systems. IBM announced that it will use Motif in some products. And Hewlett-Packard is committed to Motif, as is DEC. CAD workstation vendor Intergraph has announced plans to begin shipping Motif with its systems, and Mentor, the leading vendor of CAE tools, also plans to implement Motif across its product line.

Visix Software (Arlington, VA), a vendor of shells for Unix, has a new Motif-based desktop-manager application program called Looking Glass. The company has OEM deals to bundle the product with an X Windows software package from Interactive Systems (Santa Monica, CA) and with Intergraph's Motif-based systems. Visix will also offer Looking Glass later this year in versions for Sun, Hewlett-Packard, IBM, and DEC systems. The company had planned an Open Look version of the product as well, but, according to vice president of marketing George Hoyem, no customers have requested such a product.

The structure of both Open Look and Motif make the products very flexible. For example, Motif-based software runs fine on a non-Unix system, provided that the system has a compatible tool kit. Therefore, you can expect these graphics environments to make their way into closed system architectures.

Suppliers of graphics software and standards

For more information on graphics environments such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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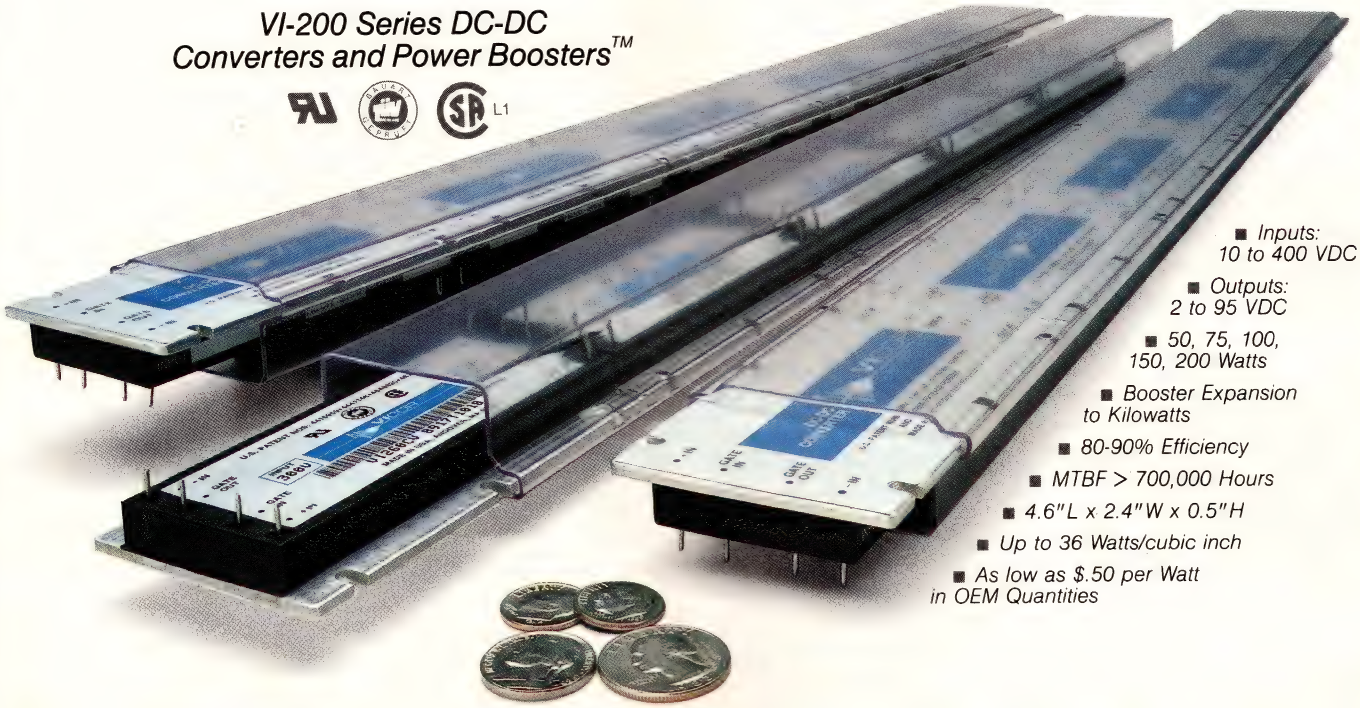

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X Windows stands out as a common base library for graphics environments and is championed by Unix International and OSF.

These graphics environments also make possible a true architecture neutral distribution format (ANDF)—one shrink-wrapped package for all systems that support X Windows. The OSF has issued an RFT for ideas on how to implement an ANDF. Potentially, a technology such as a binary or intermediate language compilation could enable independent software vendors to achieve this ANDF goal.

Already you can view technology that will be present in the next generation of graphics environments and GUIs. Hewlett-Packard's NewWave graphics environment offers an object-based GUI. The company has shipped a version for Microsoft Windows that costs $195 and plans both OS/2-PM and Motif versions. NewWave hides the native file system and presents an office metaphor based on objects, such as file folders or cabinets, or complex documents, such as spreadsheet, text-processing, or graphics application software.

Persistent links ensure updated data

NewWave maintains persistent links between objects used more than once in the system. For example, consider a complex document that includes text and graphics. NewWave lets you update the graphics within the complex document. The graphics portion of the document may also be used elsewhere in your system, for example, in another report. The persistent link makes sure that graphics components are updated anywhere else they exist in the object-oriented system, even though these components may not be active objects elsewhere.

NewWave also includes an agent facility that automatically handles fairly complex but rote chores. The package includes a training tool and perhaps the best guide to installing Windows for maximum performance ever written. To take advantage of NewWave's features, application developers have to develop new versions of their software, but according to Hewlett-Packard, a Windows-based package can easily be updated to support NewWave. Furthermore, a software vendor can ship a single version of application software to both standard Windows and Windows/NewWave users. Hewlett-Packard has gotten commitments to support NewWave from a number of Windows application developers.

Microsoft reportedly licensed much of the source code used in NewWave recently, and you may see future versions of OS/2 PM implement many NewWave-like features. The NewWave object-oriented environment offers an increase in user friendliness compared to Macintosh that is equal to the increase Macintosh offered compared to character-based MS-DOS. Therefore, user demands should fuel widespread support for NewWave or an OS/2 PM version with NewWave capabilities in the next year or two.

The future of Unix looks rosy, too. The OSF and its Motif products have sufficient backing to become an industry-wide graphics-environment standard. You'll also be able to buy NewWave for Motif within a year or two. But don't expect a shrink-wrapped version of your favorite software for heterogeneous systems on the retail shelf soon. OSF should take at least a year to settle on an ANDF implementation, and executing the chosen implementation could take much longer.

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EDN Magazine's November 9, 1989, issue will provide advanced information on Wescon/89—what you can expect at the technical sessions and what new products will be displayed at the show. Our Special Report will cover low-cost workstations—those machines that range in price from $4000 to $20,000. Other scheduled articles include

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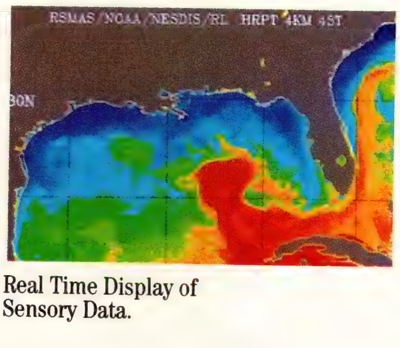

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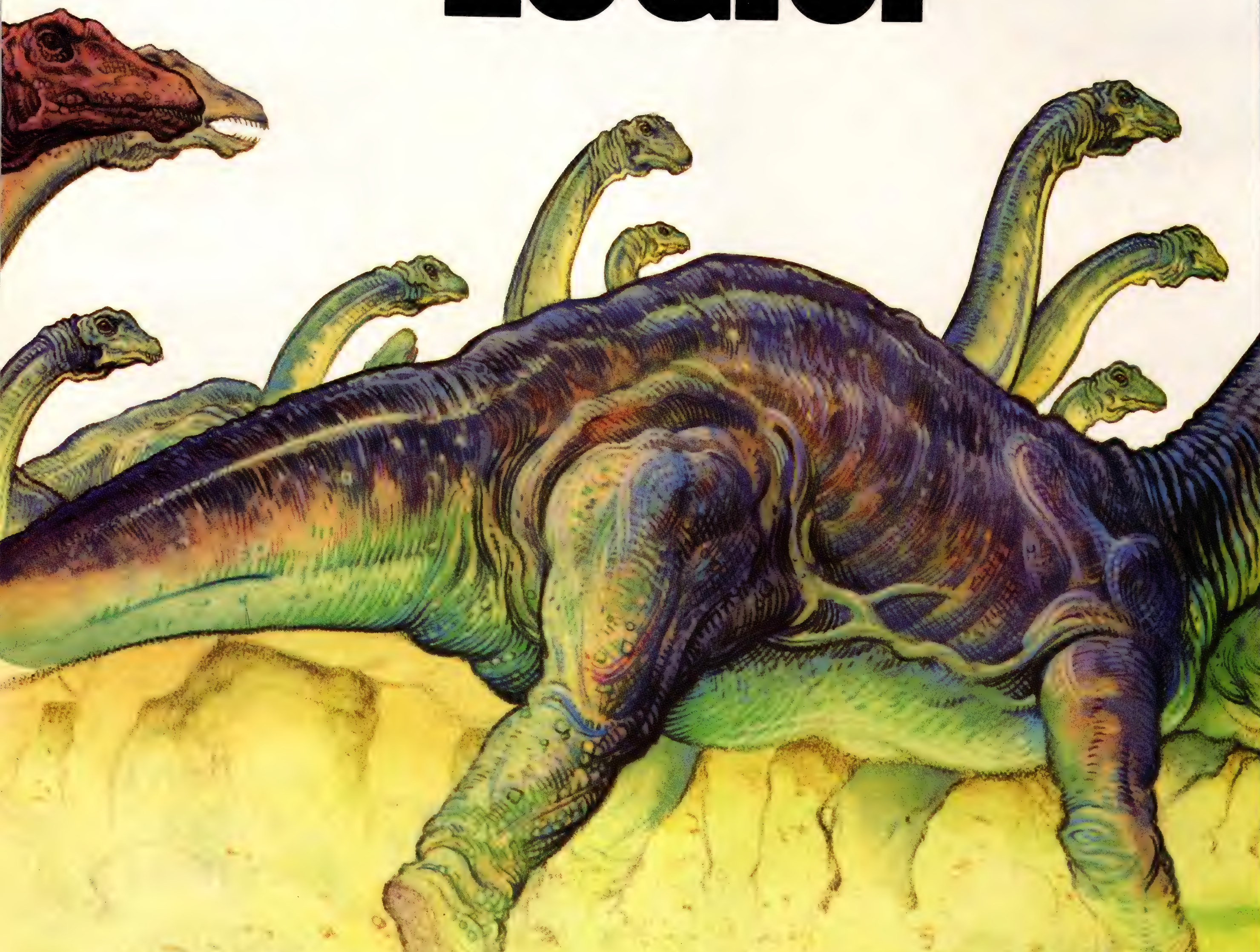

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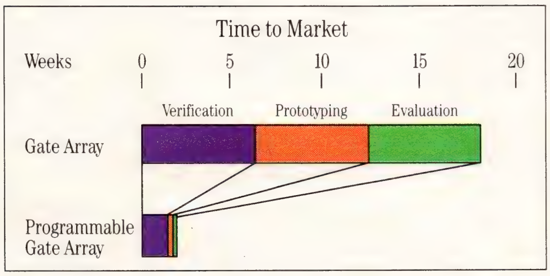

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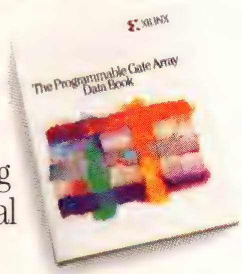

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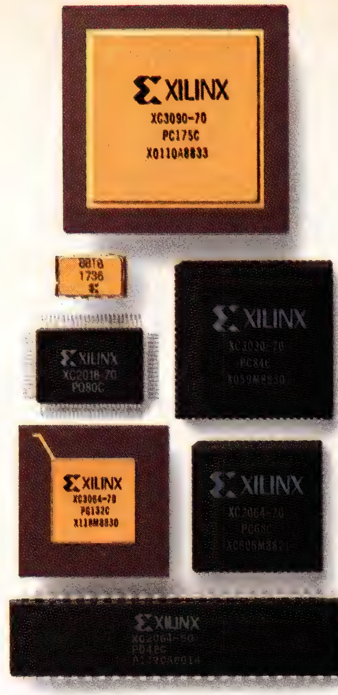

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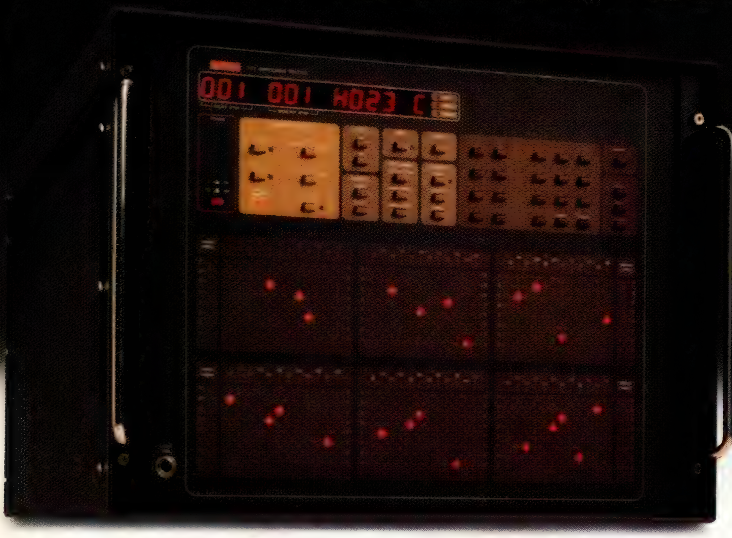

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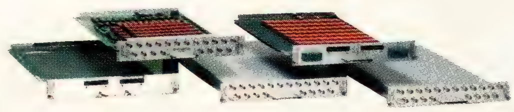

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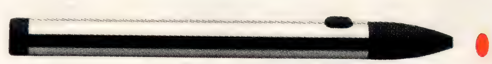

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CIRCLE NO 48

TROUBLESHOOTING

Analog Circuits

PART 12

Troubleshooting series comes to a close

In any serious troubleshooting situation, planning what tests are most likely to give you the answer quickly, rather than charging off in random directions, is usually wise. Intermittents are the toughest, most frustrating kind of troubleshooting problem. And bench instruments augment an engineer's senses and open the window of perception to the circuits he or she is troubleshooting.

Robert A Pease, *National Semiconductor Corp*

"Floobydust" is an old expression around our lab that means potpourri, catch-all, or miscellaneous. In this last installment, I'll throw into the floobydust category a collection of philosophical items, such as advice about planning your troubleshooting, and practical hints about computers and instruments.

Troubleshooting intermittent problems

The car that refuses to malfunction when you take it to the shop, the circuit that refuses to fail when you're looking at it—does it really fail *only* at 2 am?—these are the problems that require the most extreme efforts to solve.

The following techniques apply to intermittent problems:

1. Look for correlation of the problem with *something*. Does it correlate with the time of day? The line voltage? The phase of the moon? (Don't laugh.)
2. Get extra observers to help see what else may correlate with the problem. This extra help includes both *more people* to help you observe and *more equipment* to monitor more channels of information.
3. Try to make something happen. Applying heat or cold may give you a clue. Adding some vibration or mechanical shock could cause a marginal connection to open permanently.
4. Set up a storage scope or a similar data-acquisition system to trap and save the situation at the instant of the failure. Depending on the nature of the instrument, you may be able to store the data before the event's trigger or after or both.
5. Get one or more buddies to help you analyze the situation. Friends can help propose a failure mode, a scenario, or a new test that may give a clue.
6. As the problem may be *extremely* difficult, use *extreme* measures to spot it. Beg or borrow special equipment. Make duplicates of the circuit or equipment that is failing in hopes of finding more examples of the failure. In some cases, you are justified in slightly abusing the equipment in hopes of turning the intermittent problem into an all-the-time problem, which is often easier to solve.

In case you haven't guessed, I'm not a big fan of *digital* computers. When a computer tries to simulate an analog circuit, *sometimes* it does a good job; but when it doesn't, things get very sticky. Part of the

Intermittent problems require the most extreme efforts to solve.

problem is that some people put excessive confidence and belief in *anything* a computer says. Fortunately, my bosses are very skeptical people, and they agree that we must be cautious when a computer makes outrageous promises. Still, we all agree that computers promise some real advantages, if only we can overcome their adversities and problems.

In many cases, if you have trouble with the simulation of an analog system, you troubleshoot the simulation just as you would the circuit itself. You get voltage maps at various "times" and "temperatures," you insert various stimuli, watch to see what's happening, and modify or tweak the circuit just like a "real" circuit. But, just like the Mario brothers, you can encounter problems in Computerland:

1. You might have a bad circuit.
2. You might forget to ask the computer the right question.
3. You might have mistyped a value or instruction or something. The easiest mistake of this sort is to try to add a 3.3M resistor into your circuit. Spice thinks you mean 3.3 *milliohms*, not megohms. This problem has hooked almost everybody I know. I solved it by using "3300K" (3300 kΩ in Spice).
4. You might have a bad "model" for a transistor or device. I've seen a typographical error in the program listing of a transistor's model tie a project in knots for *months*.
5. You might have neglected to include strays such as substrate capacitance, pc-board capacitance, or—something that most people forget—lead inductance.
6. You might get a failure to converge or an excessive run time. Or the computer might balk because the program is taking too many iterations.

Sometimes problems happen that only a computer expert can address. But when you ask the computer guru for advice, you could get no advice or—what's worse—bad advice. After all, many computer wizards know nothing whatsoever about linear circuits. If the wizard tells me, "Hey, don't worry about that," or, "Just change the voltage resolution from 0.1 mV to 10 mV," then I must explain to the wizard that, although that advice might make some computers happy, it gives me results that are completely useless. Talking to computer wizards is sometimes difficult.

Even if you do everything right, the computer can lie to you. Then you have to make a test to prove that *you* can get the right answer and the computer can't. Then, just tell your boss that the computer has proved itself incompetent.

Photographs by Peggi Willis

***Intermittent failures**—especially those that occur only at 2 am—are the toughest to troubleshoot.*

What I really think you ought to do instead of using digital simulations is to make an analog-computer model—you'll have a lot less trouble. Be sure to scale all the capacitances at 100× or 1000× normal, so the time scale is scaled down by 100×, which makes the strays negligible. That's what I do. I will listen to alternative points of view but, be forewarned, with frosty skepticism.

There's nothing like an analog meter

Everybody *knows* that analog meters aren't as accurate as digital meters. Except . . . you can buy DVMs with a 0.8% accuracy; analog meters better than that exist. Anyway, let's detail some problems with analog meters.

Even if an analog meter is accurately calibrated at full scale, it may be less accurate at smaller signals because of nonlinearity arising from the meter's inherent imperfections in its magnetic "circuits." You can beat that problem by making your own scale to correct for those nonlinearities. Then there's the problem of friction. The better meters have a "taut-band" suspension, which has negligible friction—but most cheap meters don't. Now, as we have all learned, you can neutralize most of the effects of friction by gently rapping on, tapping at, or vibrating the meter. It's a pain in the neck, but when you're desperate, it's good to know.

Even if you don't shake, rattle, or roll your meters, you should be aware that they are position-sensitive and can give a different reading if flat or upright or turned sideways.

The worst part about analog meters is that if you drop them, any of these imperfections may greatly increase until the meter is nearly useless or dead. This

is "position sensitivity" carried to an extreme. Ideally, you would use digital meters for every purpose. But analog meters have advantages when, for example, you have to look at a trend or watch for a derivative or an amplitude peak—especially in the presence of noise, which may clutter up the readings of a digital voltmeter. So, analog meters will be with us for a long time, especially in view of their need for no extra power supply, their isolation, and their low cost.

But, beware of the impedance of meter movements. They look like a stalled motor—a few hundred millihenries—at high frequencies. But if the needle starts swinging, you'll get an inductive kick of many henries. So, if you put an analog meter in the feedback path

Methodical, logical plans ease troubleshooting

Even a simple problem with a resistive divider offers an opportunity to concoct an intelligent troubleshooting plan. Suppose you had a series string of 128 1-kΩ resistors. If you applied 5V to the top of the string and 0V to the bottom, you would expect the midpoint of the string to be at 2.5V. If it weren't 2.5V but actually 0V, you *could* start your troubleshooting by checking the voltage on each resistor, working down from the top.

But that strategy would be absurd. Checking the voltage at, say, resistor #96, then at #112 or #80, then at #120 or #104 or #88 or #72—branching along—would be much more effective. With just a few trials, you could find where a resistor was broken open or shorted to ground. Such branching along would take a lot fewer than 64 tests.

Further, if an op-amp circuit's output was pegged, you would normally check the circuit's op amp, resistors, or conductors. You wouldn't normally check the capacitors, *unless* you guessed that a shorted capacitor could cause the output to peg. Conversely, if the op amp's V_{OUT} was a few dozen millivolts in error, you might start checking the resistors for their tolerances. You might not check for an open-circuited or wrong-value capacitor, *unless* you checked the circuit's output with a scope and discovered it oscillating.

So, in any circuit, you must study the data—your "clues"—until they lead you to the final test that reveals the true cause of your problem.

Thus, you should always first formulate a hypothesis and then invent a reasonable test or series of tests, the answers to which will help narrow down the possibilities of what is bad and may, in fact, support your hypothesis. These tests should be performable. But you may define a test and then discover it is *not* performable or would be much too difficult to perform. Then I often think, "Well, if I *could* do that test, the answer would either come up 'good' or 'bad.' OK, so I can't easily run the test. But if I assume that I'd get one or the other of the answers, what would I do next to nail down the solution?"

For example, if I had to probe the first layer of metal on an IC with two layers of metal because I had neglected to bring an important node up to the second metal, I might do several other tests instead. I would do the other tests hoping that maybe I wouldn't have to do that probing, which is rather awkward even if I can "borrow" a laser to cut through all the layers of oxide. If I'm lucky, I may never have to go back and do that "very difficult or nearly impossible" test.

Of course, sometimes the actual result of a test is some completely unbelieveable answer, nothing like the answers I expected. Then I have to reconsider—where were my assumptions wrong? Where was my thinking erroneous? Or, did I take my measurements correctly? Is my technician's data really valid? That's why troubleshooting is such a challenging business—almost never boring.

On the other hand, it would be foolish for you to plan *everything* and test *nothing*. Because if you did that, you would surely plan some procedures that a quick test would show are unnecessary. That's what they call "paralysis by analysis." All things being equal, I would expect the planning and testing to require equal time. If the tests are very complicated and expensive, then the planning should be appropriately comprehensive. If the tests are simple, as in the case of the 128 resistors in series, you could make them up as you go along.

Some people put excessive confidence in anything a computer says.

of an op amp, you'll need a moderate feedback capacitor across the meter.

As I mentioned before, digital meters are *always* more accurate than analog meters . . . except for when they aren't. Recently, a manufacturer of power supplies decided to "modernize" its bench-type supplies by replacing the old analog meters with digital meters. Unfortunately, these meters came with an accuracy of ±5%. Having a 2½-digit digital panel meter (DPM) with a resolution of 1 part in 200 but an accuracy of 1 part in 20 certainly is silly. Needless to say, I stopped buying power supplies from that manufacturer.

The steadiness and irrefutability of those glowing, unwavering digits is psychologically hard to rebut. I classify the readings of the DVM or DPM with any other computer's output: You have to learn to trust a computer or instrument when it's telling the truth and to blow the whistle on it when it starts to tell something other than the truth.

For example, most slow DVMs have some kind of dual-slope or integrating conversion, so they're inherently quite linear, perhaps within 1 or 2 least-significant digits. Other DVMs claim to have the advantage of higher conversion speed; this higher speed may be of no use to the bench engineer, but it is usable when the DVM is part of an automated data-acquisition system. These faster instruments usually use a successive-approximation or recirculating-remainder conversion scheme, both of which are not inherently linear but depend on well-trimmed components for linearity. I have seen several DVMs that cost more than $1000 and were prejudiced against certain readings. One didn't like to convert 15 mV; it preferred to indicate 14 or 16.

I hate to use a DVM's autoranging mode. I have seen at least two—otherwise high-performance—DVMs that could not lock out the autorange feature. The worst aspect of these meters was that I couldn't tell where they would autorange from one range to another, so I couldn't tell where to look for their nonlinearity. After an hour of searching, I found a *couple* of missing codes at some such preposterous place as 10.18577V. And this on a $4000 DVM that the manufacturer claimed could not have such an error—could not have more than 1 ppm of nonlinearity.

Another DVM had the ability to display its own guaranteed maximum error, saying that its own error could not be more than ±0.0040% when measuring a 1-MΩ resistor. But then it started indicating that one

Spice printouts *are almost always good for something.*

of my better 1.000000-MΩ resistors was really 0.99980 MΩ. How could I prove it was lying to me? Easy—I used jiujitsu by employing its own force against itself. I got ten resistors each measuring exactly 100.000 kΩ—all the DVMs in the lab agreed on these resistors' values. When I put all 10 resistors in series, all the other meters in the lab agreed that they added up to 1.00000 MΩ; the fancy but erroneous machine said 0.99980 MΩ. Back to the manufacturer it went.

So, if you get in an argument with a digital meter, don't think that you *must* be wrong. You can usually get an opinion from another instrument to help prove where the truth lies. Don't automatically believe that a piece of "data" must be correct *just* because it's "digital."

And be sure to hold onto the user's manual that comes with the instrument. It can tell you where the guaranteed error band of the DVM gets relatively bad, such as for very low resistances, for very high resistances, and for low ac voltages.

Most digital voltmeters have a very high input impedance (~10,000 MΩ typ) for small signals. However, if you let the DVM autorange, at some level the meter will automatically change to a higher range where the input impedance becomes 10 MΩ. Some DVMs change at 2V or 3V, others at 10 or 12 or 15V, and yet others at ±20V. As I mentioned in the section on equipment, I like to work with the DVMs that stay high-impedance up to at least 15V. But, the important thing is to know the voltage at which the impedance changes. A friend reminded me that a guy he knows had recently taken a week's worth of data that had to be retaken because

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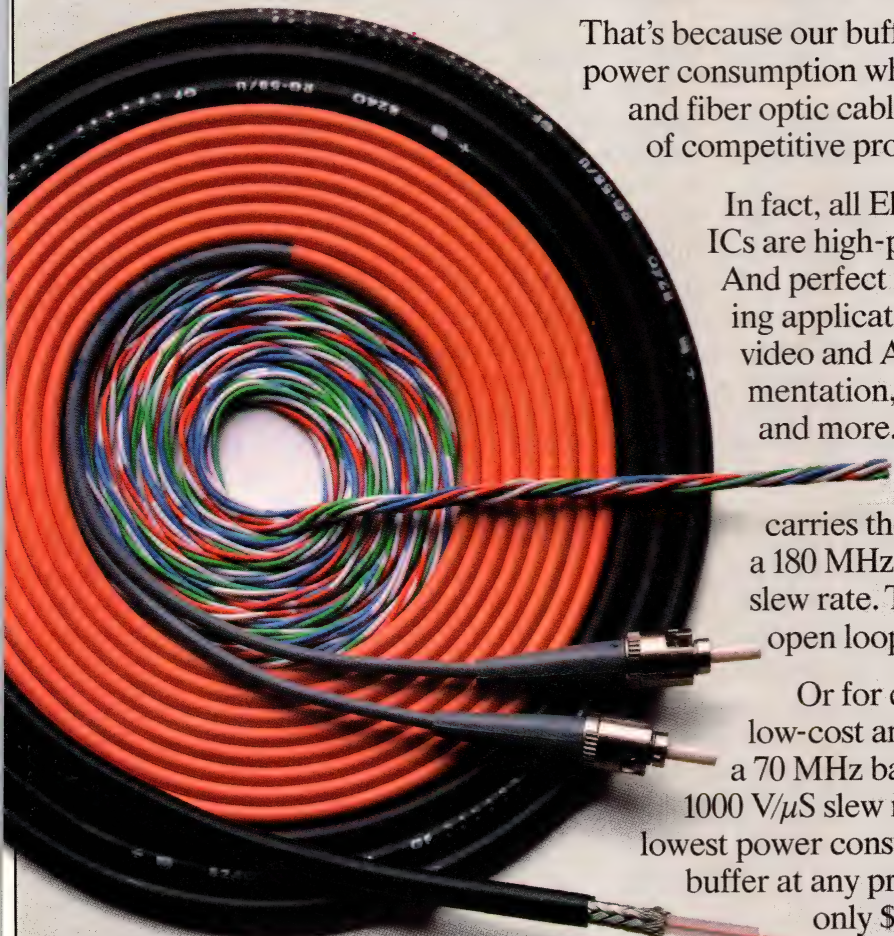

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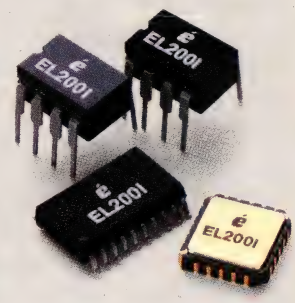

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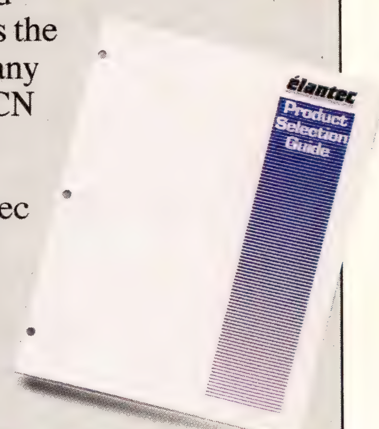

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In some cases, you are justified in slightly abusing equipment in the hopes of turning an intermittent problem into an all-the-time problem.

he neglected to allow for the change of impedance. I think I'll go around our lab and put labels on each DVM.

Still, DVMs are very powerful and useful instruments, often with excellent accuracy and tremendous linearity and resolution—often as good as 1 ppm. I've counted some of these ultralinear meters as my friends for many years. I really do like machines that are inherently, repeatedly linear.

One picky little detail: Even the best DVM is still subject to the adage, "Heat is the enemy of precision." For example, some DVMs have a few extra microvolts of warm-up drift, but *only* when you stand the box on its end or side. Some of them have a few microvolts of thermal wobble and wander when connected to a zero-volt signal (shorted leads), but *only* when you use banana plugs or heavy-gauge (16, 18, or 20 gauge) leads—not when you use fine wire (26 or 28 gauge). The fine-wired leads do not draw as much heat from the front-panel binding posts. So, even the best DVM auto-zero circuit cannot correct for drifts outside its domain.

Most engineers know that DVMs add a resistive (10-MΩ) load to your circuit and a capacitive load (50 to 1000 pF) that may cause your circuit to oscillate. But, what's not as well known is that even the better DVMs may pump noise back through their input terminals and spray a little clock noise around your lab. So if you have a sensitive circuit that seems to be picking up a lot of noise from *somewhere*, turn off your DVM for a few seconds to see if the DVM is the culprit. If that's not it, turn off the function generator or the soldering iron.

Signal sources

While I'm on the subject of instruments, I really enjoy using a good function generator to put out sines and triangle waves and square waves and pulses. But I certainly don't expect the signals to be undistorted—all these waveforms will distort, especially at high frequencies. So if I want my function generator to give me a clean sine wave, I put its output through an active filter at low frequencies or an LC filter at high frequencies. If I want a clean, crisp square wave, I will put the signal through a clipping amplifier or into a diode-limited attenuator **(Fig 1)**. If I want a cleaner triangle than the function generator will give me, I just make a signal generator from scratch.

A function generator lets me down when some absent-minded person pushes one button too many and the output stops. It can take me five minutes to find what the problems are. I love all those powerful versatile functions when I need them, but they drive me nuts when the wrong button gets pushed.

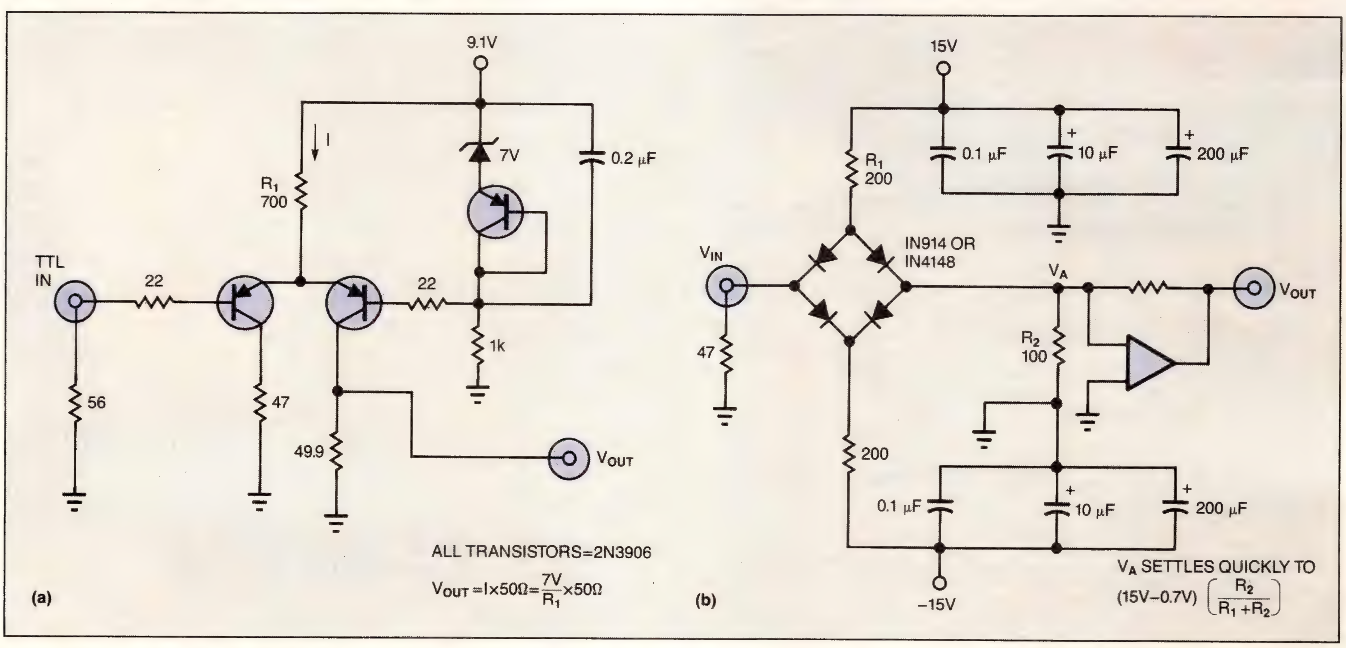

***Fig 1—Either a clipping amplifier (a)** or diode-limited bridge **(b)** will give you a clean, crisp square wave.*

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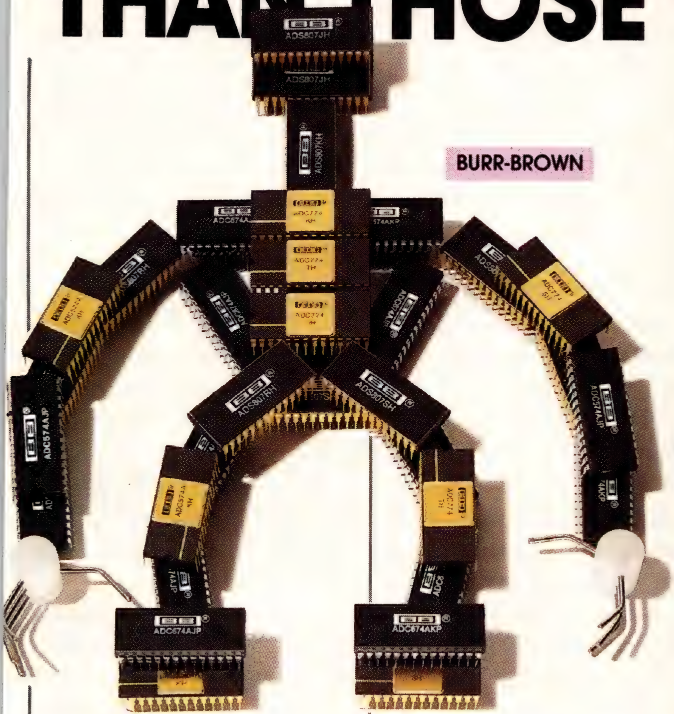

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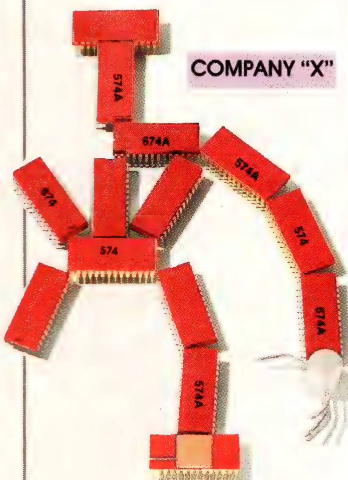

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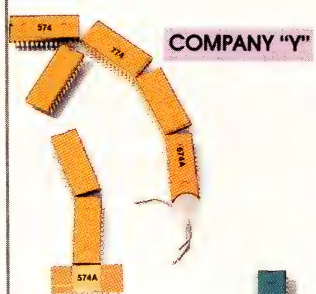

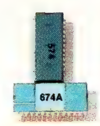

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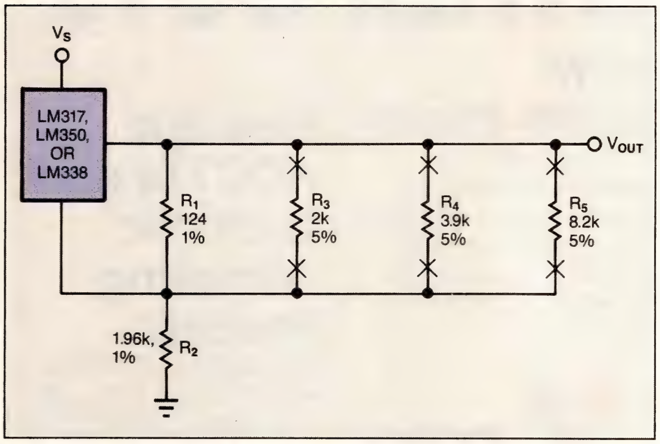

***Fig 2—If you're worried that some foolish person** will ruin a circuit by misadjusting a trimming potentiometer, you can foil the bungler with this "snip-trim" network. The procedure for trimming V_{OUT} to 22V within 1% tolerance is as follows: If V_{OUT} is higher than 23.080V, snip out R_3 (if not, don't); then if V_{OUT} is higher than 22.470V, snip out R_4 (if not, don't); then if V_{OUT} is higher than 22.160V, snip out R_5 (if not, don't). Obviously, you can adapt this scheme to almost any output voltage. Choosing the breakpoints and resistor values is only a little bit tricky.*

Similarly, a scope's trace can get lost and hide in the corner and sulk for many minutes on end if you don't realize that somebody (maybe your very own errant fat finger) pushed a treacherous button. When the digital scopes with their multiple layers of menus and submenus start playing that game, I find I need a buddy system—somebody to come and bail me out when I get hopelessly stuck. What *menu* is that dratted beamfinder on, anyway?

But, scopes work awfully well these days. Just don't expect precision results after you drive the trace many centimeters off scale by turning up the gain to look at the bottom of a tall square wave. Scopes aren't obligated to do that very well. Similarly, be sure to keep the trimmers on your 10× probes well adjusted, and run a short ground path to your probes when you want to look at fast signals.

How to trim without trimming potentiometers

Speaking of keeping circuits well trimmed, some people like to use trimming potentiometers to get a circuit trimmed "just right." Other people hate to because the potentiometers are expensive or unreliable or drifty. Worst of all, if a circuit can be trimmed, it can also be mistrimmed; some person may absent-mindedly or misguidedly turn the potentiometer to one end of its range or to the wrong setting. How long will it take before that error is corrected?

For just this reason, some people prefer fixed-voltage regulators because they always have a valid output (±5%) and can never get goofed up by a trimming potentiometer. Other people need a tighter tolerance yet are nervous about the trimming potentiometer. You will find the solution in the snip-trim network in **Fig 2.** This scheme will let you trim a regulator well within 1% without trimming potentiometers. Note that you could also use this technique to set the gain of integrators and the offset of amplifiers. It's not always easy to engineer the correct values for these trims, but it is possible. And, nobody's going to go back and *tweak* the potentiometer and cause trouble if there's no potentiometer there to tweak.

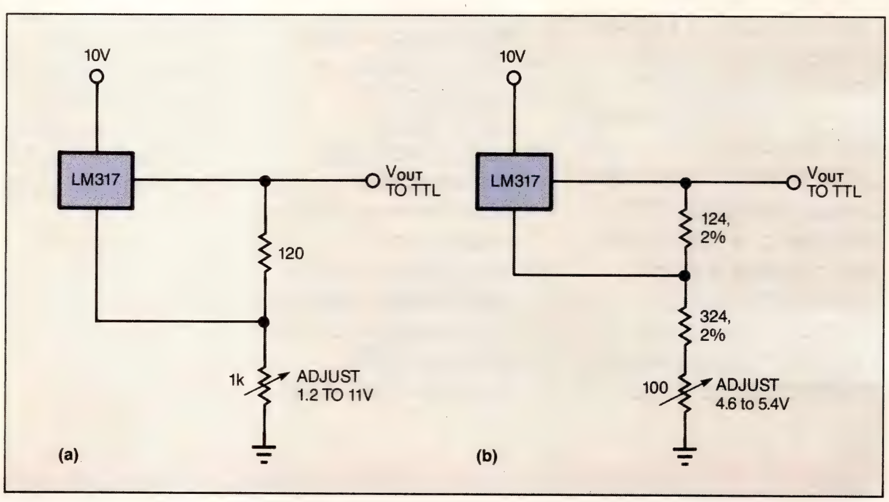

***Fig 3—You can avoid incurring Bob's ire** if you dodge one of his pet peeves: an excessive trimming-potentiometer adjustment range **(a)**. The circuit in **b** suits TTL much better.*

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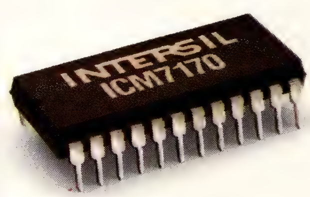

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A pet gripe of mine concerns engineers who design a circuit with an adjust range that's so wide that damage can occur. For example, **Fig 3a** is a bad idea for a regulator for a 5V supply for TTL because the TTL parts would be damaged if someone tweaks the pot to one end of its range. **Fig 3b** is better.

In closing, let's all work together lest troubleshooting become a lost art. I've done my bit, now you do yours. Send your own troubleshooting articles to EDN. If you don't have enough troubleshooting ideas to produce a full-length article but do have some good tips that you didn't see in this series, send them to EDN's Design Ideas editor. No doubt, EDN will print some of them. Please send me a copy of anything you send to EDN—I'd love to look at it. And if you've got any comments about *my* series, please write to me at National Semiconductor Corp, M/S C2500, Box 58090, Santa Clara, CA 95052. After all the tips I've given you, it's only fair that you share your comments with me. **EDN**

Author's biography

For more information about Bob Pease, see the **box,** *"Who is Bob Pease, anyway?" on page 148 of the January 5, 1989, edition of EDN.*

Acknowledgments

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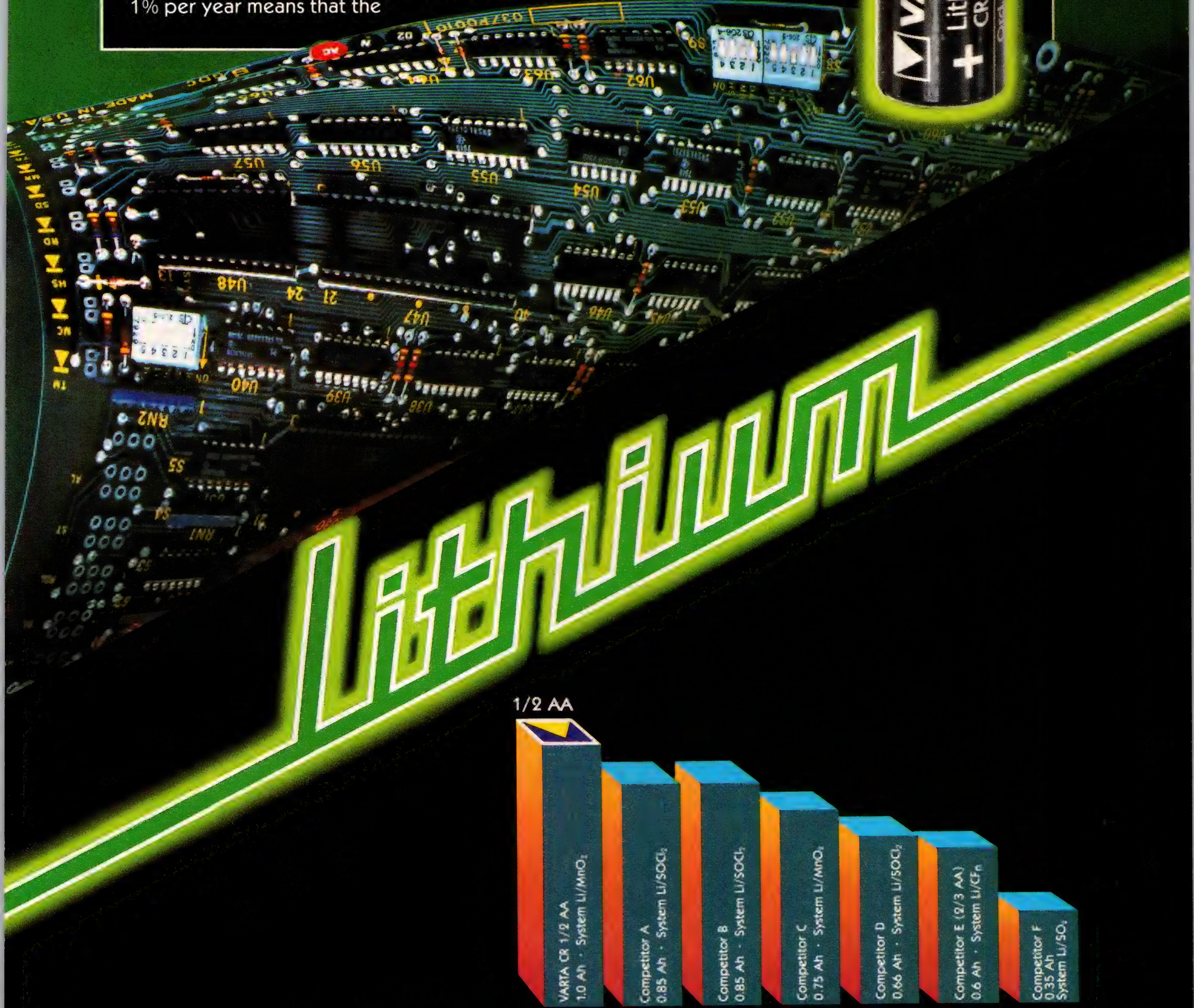

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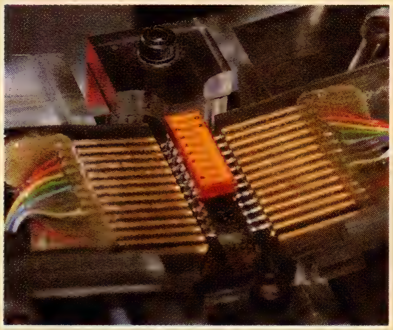

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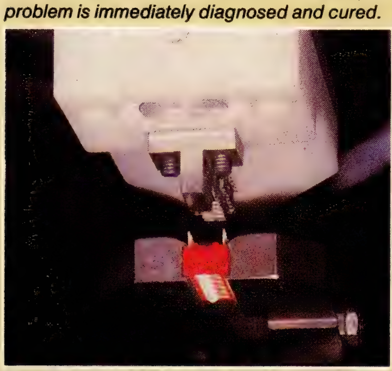

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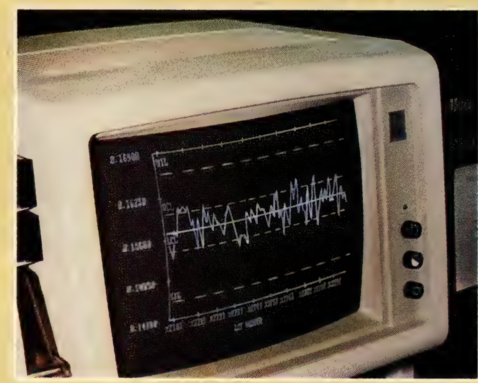

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Rate-monotonic scheduling ensures tasks meet deadlines

Traditional approaches to creating multitasking systems can force you to overdesign your hardware to ensure that all critical software tasks will meet their hard deadlines. Rate-monotonic scheduling, a simple priority-setting method, lets you guarantee that all tasks will meet their deadlines and that an overloaded system won't crash.

Lee Silverthorn, *DDC-I Inc*

Rate-monotonic scheduling is a technique that lets you prioritize tasks for a real-time, multitasking kernel and prove mathematically that your system will meet all of its critical deadlines. In addition, this scheduling approach lets you design a system that, when overloaded, will fail gracefully instead of crashing.

In real-time systems, periodic tasks perform repetitive work. Two parameters completely describe a periodic task's performance requirements: the task's execution time and its execution period. The execution time is simply the amount of processor time the task requires for each execution. The execution period is the time between succeeding initiations of that task. You can determine the load a task places on the system processor by dividing the execution time by the execution period (effectively multiplying the execution time by the execution frequency).

A cyclic executive is the simplest approach to building real-time software systems that execute periodic tasks. The executive consists of a software loop that executes a fixed list of tasks (**Fig 1**). The core of the executive need be little more than a small program that calls each task in turn via a jump table that contains a list of task addresses. Task service is deterministic: every task is executed when its turn in the loop comes around. If a task has nothing to do it terminates itself quickly, but a portion of every task is still executed each time through the loop.

Cyclic executives are very simple to create because they don't rely on interrupts or other forms of exception processing. However, cyclic executives can have poor response times when responding to external events because an event can't be handled until the executive calls the appropriate service routine—and that may require almost an entire pass through the software loop. Also, any change to the cyclic executive or to the routines it calls alters the software loop's timing, so the cyclic executive may prove inflexible and difficult to modify if your system specifications change.

A cyclic executive will satisfy your application's needs if the entire software loop executes in less time than the most frequently executed task's execution period. However, if the loop's execution time exceeds the required period of one of your periodic tasks, you

Rate-monotonic scheduling allows you to prove mathematically that your system will meet all of its critical deadlines.

may have to replicate that particular task two or more times within the loop in order to meet that task's deadlines.

When you design a cyclic executive's software loop, you must calculate the loop's period on the basis of the maximum time required to execute every task, including all the tasks that service exceptions. Naturally, if you create tasks that have variable execution times, you greatly complicate the loop's timing calculations. In addition, you may run into performance problems with a cyclic executive after you finish your initial product design. Changes that you make to the software during debugging or maintenance, such as modifications to existing tasks or the addition of new tasks, can alter the software loop's timing so that periodic tasks can no longer meet their critical deadlines. To solve this problem, you may be forced to use a faster, more powerful processor, but this solution is unsatisfactory because it increases your hardware costs.

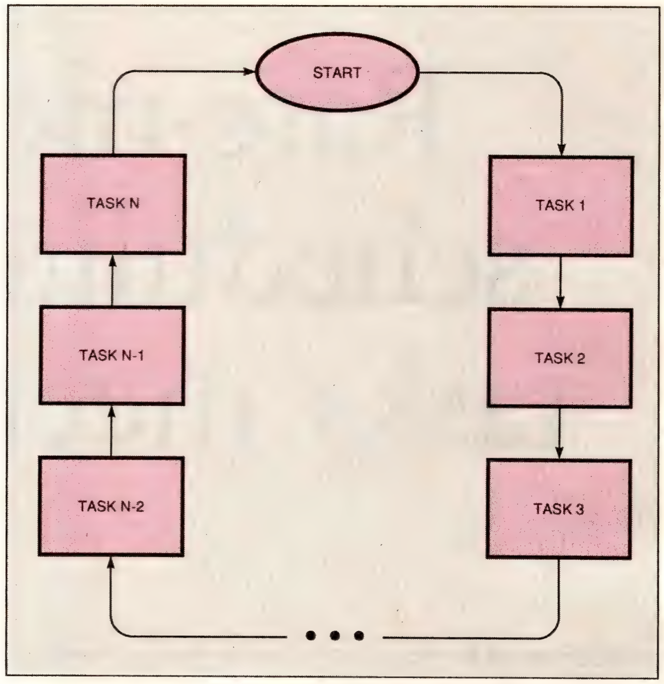

***Fig 1—A cyclic executive executes every system task** using a simple software loop. For every pass through the loop, each task is executed once.*

Interrupts avoid overbuilt systems

If you're faced with a task load that can't run on the processor you want to use, consider using an interrupt-driven, real-time, multitasking kernel. Instead of executing a fixed list of tasks, this type of kernel relies on hardware or software interrupts to schedule tasks. If you don't care exactly when a particular task is executed, as long as you meet that task's deadline, you often won't need the deterministic feature of the cyclic executive. A software design based on a multitasking kernel probably won't need to execute every possible task in a certain time period. Instead, the system services only the tasks that request service, and therefore, during normal operation, it needs less processing power than does a cyclic executive.

You must assign priorities to tasks running under a multitasking kernel so that the kernel can know which task to execute first if more than one task requires service. Using an ad hoc priority-assignment scheme, you often set task priorities so that the most critical tasks have higher priority than the others. This approach to setting priorities feels right intuitively, but it doesn't let you prove that your system will work under all conditions. Also, this approach doesn't allow you to predict your system's performance under overload conditions.

Rate-monotonic scheduling allows you to set task priorities for systems that are based on a multitasking, real-time kernel, and to prove that your software design will meet hard deadlines for critical tasks. The technique is based on some statistical research performed at the Department of Computer Science at Carnegie-Mellon University (CMU) and the Software Engineering Institute at CMU (**Ref 1**). Rate-monotonic scheduling (RMS) makes two assumptions:

- A simple, real-time system design consists of a number of independent periodic tasks that execute under the control of a pre-emptive scheduler. Tasks are independent if the scheduler doesn't have to synchronize their execution.
- The time required to execute a particular task is constant. If the task duration is variable, you can use the worst-case number instead.

If these assumptions are valid for your application, the theory allows you to calculate a theoretical safe upper bound for processor loading. All tasks will meet their critical deadlines as long as the actual processor load is below this theoretical bound. Note **Theorem 1**:

$$\text{Safe upper bound} = n(2^{(1/n)}-1),$$

where n represents the number of tasks the system must execute. **Table 1** lists safe loads for systems that execute one to nine tasks. The worst-case safe upper bound for processor loading occurs when the number

of tasks approaches infinity and converges to ln(2), or 69%.

Fig 2 plots the probability of missed deadlines for a uniformly distributed set of periodic tasks on the basis of three scheduling algorithms. The FIFO algorithm is by far the worst, causing missed deadlines at a paltry 5% processor utilization for the worst-case task set. Arbitrary scheduling is almost as bad as the FIFO method. However, rate-monotonic scheduling allows all tasks to meet hard deadlines at least until processor utilization exceeds the worst-case bound of 69%. **Fig 2** is based on statistical simulations (**Ref 2**).

The maximum processor-load estimate of 69% is based on a worst-case set of tasks for a hypothetical system and is, therefore, very pessimistic. Additional research into rate-monotonic scheduling shows that most systems can operate safely at much higher processor loadings than those suggested by the worst-case number; in fact, the research indicates that real multitasking systems can safely attain processor utilizations as high as 88% (**Ref 3**). In addition, **Ref 3** gives you a second theorem that lets you compute whether a specific set of independent periodic tasks, prioritized by the rate-monotonic scheduling algorithm, can or can't always meet its deadlines. Thus, you needn't use the worst-case limits if you know the execution times and periods for all the tasks to be scheduled. For a set of n tasks, **Theorem 2 states:**

$$\sum_{j=1}^{n} f_{ceil}\,[lT_k/T_j]C_j <= lT_k$$

where j, k, and l are integers and f_{ceil} is the ceiling function that returns the whole number greater than or equal to its argument. If at least one of the equations generated by **Theorem 2** is true, then the task set can be scheduled.

For most real-time applications, you can generate the specific information you need to compute whether a set of real-time tasks can be scheduled using **Theorem 2**. In effect, you must act as a scheduler to determine how many tasks will be executed by each scheduling point. The scheduling points for any given task occur at that task's deadline and at the ends of the periods of all the higher-priority tasks that are executed before that deadline.

The set of equations generated by **Theorem 2** is too tedious to solve by hand; however, **Listing 1** and **Listing 2** provide you with two versions, written in Basic and Ada respectively, of a program that makes the work much easier. The program accepts a list of tasks, with their execution times and periods, and computes each of the scheduling points up to the hard deadline of the least important, lowest frequency task. You should enter the tasks in order, starting with the most frequent and ending with the the least frequent. If it can schedule all periodic tasks within that period, the program informs you of its success. If the program can't schedule all of the tasks, however, it warns you that your design may fail.

TABLE 1—SAFE PROCESSOR LOAD VS NUMBER OF INDEPENDENT TASKS

NUMBER OF TASKS	SAFE UPPER BOUND
1	1.000
2	0.828
3	0.779
4	0.756
5	0.743
6	0.734
7	0.728
8	0.724
9	0.720

Rate-monotonic scheduling is easy to apply

Once you get past the mathematical analysis and statistical simulations that prove the theory, rate-monotonic scheduling becomes an incredibly easy technique to apply. To use the rate-monotonic-scheduling algorithm for a system comprising several independent

Text continued on pg 196

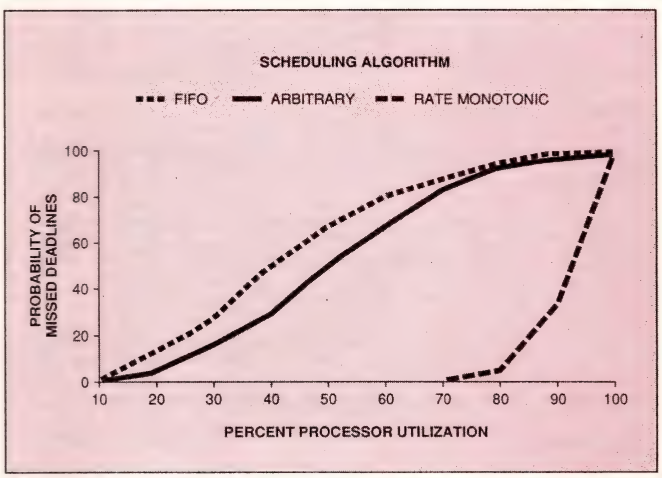

Fig 2—At any realistic processor loading, *FIFO and arbitrary task-scheduling techniques face the very real problem of missing their deadlines. Rate-monotonic scheduling, in contrast, allows you to safely achieve much higher processor loadings with your real-time software designs.*

LISTING 1 — A BASIC PROGRAM TO CHECK HARD DEADLINES

```
200 REM
210 REM The following four lines make the program read better
220 OPTION BASE 1
230 TASKTIME = 1
240 TASKPERIOD = 2
250 U=0
260 REM
270 REM Collect the task information
280 REM
290 INPUT "Enter the number of tasks to schedule ", NTASKS
300 PRINT
310 DIM TASKS[NTASKS,2]
320 FOR I=1 TO NTASKS
330   PRINT "Enter the execution time for task "; I;" in milliseconds";
340   INPUT C
350   PRINT
360   PRINT "Enter the execution period for task "; I;" in milliseconds";
370   INPUT T
380   PRINT
390   U = U + C/T
400   TASKS[I,TASKTIME]=C
410   TASKS[I,TASKPERIOD]=T
420 NEXT I
430 REM
440 REM Check to see if tasks are schedulable under theorem 1
450 REM
460 IF U > NTASKS * (2^(1/NTASKS) - 1) THEN GOTO 500
470 PRINT "Tasks are schedulable under theorem 1"
480 END
490 REM
500 REM Now check each scheduling point out to Tn
510 REM
520 FOR L=1 TO NTASKS
530   FOR K=1 TO NTASKS
540     UTILIZATION = 0
550     FOR J=1 TO NTASKS
560       TEMP = L * TASKS[K,TASKPERIOD] / TASKS[J,TASKPERIOD]
570       REM
580       REM Fake the ceiling function
590       REM
600       CEILING = INT(TEMP)
610       IF CEILING < TEMP THEN CEILING = CEILING + 1
620       UTILIZATION = UTILIZATION + CEILING * TASKS[J,TASKTIME]
630     NEXT J
640     SCHEDULEPOINT = L * TASKS[K,TASKPERIOD]
650     REM
660     REM Check to see if this schedule point is too late
670     REM
680     IF SCHEDULEPOINT > TASKS[NTASKS,TASKPERIOD] THEN 780
690     REM
700     REM Schedule point is not too late, check utilization
710     REM
720     PRINT "For l =";L;" and k =";K;" utilization is "; UTILIZATION
730     PRINT "Schedule point is "; SCHEDULEPOINT;
740     IF UTILIZATION<=SCHEDULEPOINT THEN SUCCESS = 1
750     IF UTILIZATION<=SCHEDULEPOINT THEN PRINT ", SUCCESS!" ELSE PRINT ", FAIL"
760     PRINT
770     IF SUCCESS = 1 THEN END
780   NEXT K
790 NEXT L
800 PRINT "Sorry, these tasks may not meet their deadlines"
810 END
```

LISTING 2 — AN ADA PROGRAM TO CHECK HARD DEADLINES

```
with TEXT_IO;     use TEXT_IO;
with MATH_PACK;   use MATH_PACK;
procedure RMS_CHECK is

  NTASKS : integer;

  package INT_IO is new INTEGER_IO(integer);
  package FLT_IO is new FLOAT_IO(float);

  function INPUT_AND_CHECK_RMS (NTASKS :  integer) return boolean is

    subtype  TASK_RANGE is integer range 1..100;

    type TASK_CHARACTERISTICS is (TaskTime, TaskPeriod);

    type TASK_INFO is array (TASK_RANGE, TASK_CHARACTERISTICS)
                              of Float;

    TASKS : TASK_INFO;
```

LISTING 2 — AN ADA PROGRAM TO CHECK HARD DEADLINES —continued

```
    TEMP          : float;
    U             : Float := 0.0;
    UTILIZATION   : Float := 0.0;
    SCHEDULEPOINT : Float := 0.0;
    CEILING       : integer;

  begin

    -- Collect the task information

    for I in 1 .. NTASKS loop
    new_line;
    put("Enter the execution time for task" & integer'image(I)
          & " in milliseconds (X.X): ");
    FLT_IO.get(TASKS(I,TaskTime));

    new_line;
    put("Enter the execution period for task" & integer'image(I)
          & " in milliseconds (X.X): ");
    FLT_IO.get(TASKS(I,TaskPeriod));

    U := U + TASKS(I,TaskTime) / TASKS(I,TaskPeriod);
  end loop;

  -- Check to see if tasks are schedulable under Theorem 1

  if U <= float(NTASKS) * (exp((1.0/float(ntasks)), 2.0) - 1.0) then
    new_line;
    put_line("Tasks are schedulable under Theorem 1 ");
    return true;
  end if;

  -- Check each scheduling point out to Tn

  for L in 1 .. NTASKS loop
    for K in 1 .. NTASKS loop

      UTILIZATION := 0.0;

      for J in 1 .. NTASKS loop
        TEMP := float(L) * TASKS(K,TaskPeriod) / TASKS(J,TaskPeriod);

        -- Fake the Ceiling function

        CEILING := Integer(Temp);

        if float(CEILING) < TEMP then
          Ceiling := Ceiling + 1;
        end if;

        UTILIZATION := UTILIZATION + float(CEILING) * TASKS(J,TaskTime);
      end loop;

      SCHEDULEPOINT := float(L) * TASKS(K,TaskPeriod);

      -- Check to see if this schedule point is too late

      if SCHEDULEPOINT <= TASKS(NTASKS,TaskPeriod) then
        -- Schedule point is not too late;  check utilization
        new_line;
            put("For L = " & integer'image(L) & " and K = " & integer'image(K)
                  & " utilization is ");
            FLT_IO.put(UTILIZATION);
            new_line;
            put("Schedule point is ");
            FLT_IO.put(Schedulepoint);
            new_line;

            if UTILIZATION <= SCHEDULEPOINT then
              put("Success!");
              return true;
            end if;
          end if;
        end loop;
      end loop;
      return false;
    end INPUT_AND_CHECK_RMS;

  begin
    new_line;
    put ("Enter the number of tasks to schedule: ");
    INT_IO.get (NTASKS);
    if not INPUT_AND_CHECK_RMS (NTASKS) then
      put_line("These tasks may not meet their deadlines");
    end if;
  end RMS_CHECK;
```

A cyclic executive's scheduling strategy is simple: it executes every system task each time through the loop.

periodic tasks, you simply set the task priorities in decreasing order of task execution period. Thus, the most frequently executed task gets the highest priority, and the least frequently executed task gets the lowest. Tasks with intermediate execution rates receive intermediate priorities. That's the entire prioritization algorithm.

Use a pre-emptive scheduler

To make proper use of the prioritization that rate-monotonic scheduling dictates, your multitasking kernel must employ a pre-emptive scheduler—one that allows higher-priority tasks to interrupt the execution of tasks with lower priority. The scheduler must maintain an ordered list of tasks that require service, basing the order on task priority. Your system must also incorporate one or more interval timers that alert the scheduler when each task's activation time arrives.

A gyroscopic position-display system is a simple example of a system that might employ rate-monotonic scheduling (**Fig 3**). The tasks in this system consist of sampling the gyroscope, updating the position information stored in memory, calculating the change in position, and displaying the position information. In this example, gyroscope sampling requires the most frequent execution, and display updates occur least frequently. Each task must run once within each of its execution periods. As long as a task executes during each of its execution periods, it will meet all of its deadlines. Note that a task's execution time *must* be shorter than its execution period or it will *never* meet its deadlines.

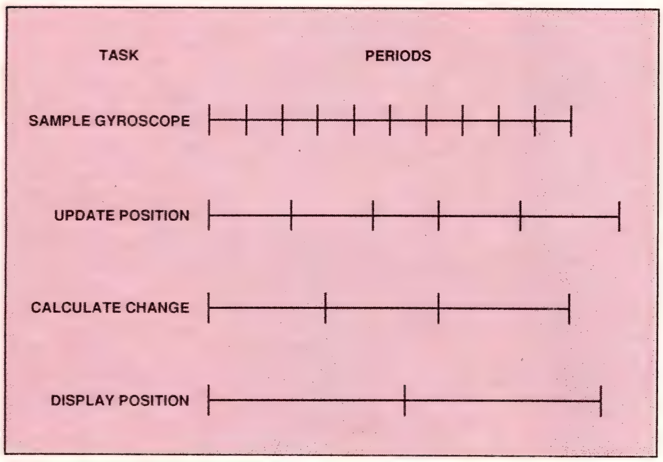

Fig 3—These tasks for a gyroscopically-controlled position display, *which are typical of tasks found in many real-time systems, must be executed periodically with varying frequencies.*

TABLE 2—RATE-MONOTONIC ALGORITHM EXAMPLE: EXECUTION TIMES AND PERIODS

PERIODIC TASK	EXECUTION TIME (C) (MSEC)	EXECUTION PERIOD (P) (MSEC)	UTILIZATION (U = C/P)
SAMPLE GYROSCOPE	0.6	3	0.2
CALCULATE GYROSCOPE CHANGE	5.2	13	0.4
UPDATE POSITION	0.7	7	0.1
DISPLAY POSITION	2	20	0.1
		TOTAL UTILIZATION =	0.8

The execution times and periods for the four tasks in the gyroscopic position-display example appear in **Table 2**. In this simplified example, task-switching times are included in the corresponding task-execution times, but you can also use the rate-monotonic scheduling algorithm to schedule an explicit task-switching task in addition to the other tasks.

You can compute an individual task's utilization factor (U) by dividing the task's execution time by its execution period. In this example, the total processor load is 80%, calculated by adding up the system's individual-task utilization factors. The load exceeds the maximum safe utilization of 75.6% for a 4-task system as computed by **Theorem 1** and listed in **Table 1**. Therefore, the system in this example might slip some task deadlines. Rate-monotonic theory doesn't tell you that this system *will* fail; it warns you that it *might* fail. However, running the hard-deadline program to check the ability of the display-position task to meet its deadline shows that *all* tasks in this example will always meet their hard deadlines.

Failing gracefully

Suppose we modify this example slightly by assuming that the position-display task in the example system has a 4-msec execution time. This change raises that task's processor utilization to 20% and increases the total processor utilization to 90%. Now, both the safe-upper-bound calculations and the hard-deadline program indicate that the set of four tasks aren't guaranteed to meet all of the tasks' hard deadlines. However, this sample system might still meet your specifications if it could consider the lowest priority task as noncritical. Thus, if the position-display task (with a 4-msec execution time) could occasionally slip its 20-

msec deadline without seriously degrading the system's performance, then that task's processor load would no longer be part of the total load for critical tasks.

In this case, eliminating the 20% processor load imposed by the extended (but no longer critical) position-display task reduces the critical processor load to 70%, which is safely below **Theorem 1's** bound calculation. Therefore, rate-monotonic scheduling guarantees that all tasks, excluding the 4-msec position-display task, will always meet their respective deadlines. To design a system that will fail gracefully, set the priorities of

Rate-monotonic scheduling and Ada

The definition of the Ada programming language supports concurrent tasking through the rendezvous mechanism, making Ada an excellent candidate for creating real-time systems based on rate-monotonic scheduling. Unfortunately, rate-monotonic scheduling assumes that high-priority tasks can pre-empt tasks with lower priority and that low-priority tasks can't block tasks with higher priority for unreasonable periods of time. The blocking of a high-priority task by a lower-priority task is called priority inversion, and the current Ada standard allows unbounded priority inversion. However, an Ada compiler and its associated runtime system can support rate-monotonic scheduling if they incorporate certain design features. In fact, you can overcome all of the problems associated with priority inversion in Ada programs and still comply with Ada's official definition.

One problem associated with priority inversion involves the different operating modes that many real-time systems must support. For example, the positioning of an airplane's control surfaces is far more critical at supersonic speeds than when the plane is flying at a slower speed. If the task that controls these control surfaces always has a high priority, however, the system's processor allocates an unnecessary amount of time to that task when the plane isn't flying fast. Dynamic task priorities, which can be changed by an executing program, avoid this problem by letting a real-time system alter task priorities to match the system's current operating mode.

Another potential source of priority inversion stems from Ada's task server, a special type of task that selects and executes other tasks. Ada's definition says that a Select statement can choose arbitrarily from several alternative tasks. If that selection isn't based on task priorities, a priority inversion can occur. However, you can prevent a priority inversion and satisfy the Ada definition by basing task selection on the priorities of the alternative tasks, so that the highest priority task is picked.

An Ada program can also assign priorities to task servers, because they are tasks. Priority inversion can occur if a task server with low priority is pre-empted by an independent intermediate-priority task before the server is able to execute a high-priority task. A system that employs task servers can avoid priority inversions in this situation, however, if the server inherits the maximum priority of all tasks requesting service.

Task servers present yet another problem that can cause priority inversion. Ada's definition requires requests to a server by associated tasks to be served in FIFO order, regardless of priority. A FIFO queue allows a low-priority task to block a high-priority task, causing a priority inversion. However, if a task server executes tasks according to a schedule based on task priority, rather than on the FIFO queue's arrival-time scheme, no inversion will occur.

Along with its validated Ada compiler system, DDC-I Inc includes an alternate Ada runtime executive that supports rate-monotonic scheduling by implementing dynamic task priorities, task selection based on task priority, priority inheritance for task servers, and server queues that order tasks based on priority. This alternate runtime system correctly executes the entire Ada test suite of validation programs. The Ada compiler produces the same code for either the standard or the alternate executive—you select the desired executive with a linker switch. DDC-I has also validated its runtime executive, which supports rate-monotonic scheduling.

Once you get past the mathematical analysis and statistical simulations that prove the theory, rate-monotonic scheduling is incredibly easy to apply.

noncritical tasks below the priorities of critical tasks and use the rate-monotonic scheduling theorems to ensure that critical tasks will always meet their deadlines.

Importance and priority aren't identical

Many experienced software designers, when first exposed to rate-monotonic scheduling, object to the technique because it seems to ignore the "real" priorities of tasks. Certain jobs, such as life-support functions, obviously are more important than others and therefore intuitively have higher priority. However, a priority is merely a number for the multitasking kernel to use when making scheduling decisions and doesn't necessarily indicate the task's importance to the overall system performance. Rate-monotonic scheduling lets you schedule tasks to ensure timely execution of all critical tasks. If, when using this method, you can guarantee that the life-support functions will always be executed by the required deadlines, you shouldn't really care what priority the algorithm assigns to the task.

Blasting through bottlenecks

The rate-monotonic scheduling technique also points out critical sections of code that limit your system's performance. If you reduce the processor utilization of the highest priority task, either by using a faster processor or by rewriting the task so that it runs faster, you make more processor time available to the other tasks without substantially changing the maximum safe processor load for your system. Once you've improved the performance of the highest priority task, you can work on improving the execution time of the task with the second highest priority, and so on; at each level, a reduction of execution time makes a little more time available for the remaining lower-priority tasks. Note that improving the performance of the task with the lowest priority helps only that specific task.

Table 3 again catalogs the four tasks in the position-display example, but it lists three different priorities for each task. The first set of numbers is the intuitive importance of the task, from most important (1) to least important (4) with regard to the product's mission. The order might be based on a designer's gut feeling for the relative importance of each task or might even be based on the system's specifications. In this example, the designer attributes the greatest importance to the task that calculates the change in the gyroscope reading.

The second column in **Table 3** simply inverts the numbers in the first column, giving the "most important" task the largest number (4) to indicate that this task should have topmost priority to the multitasking kernel. A multitasking system based on this set of priorities will fail immediately, because the 5.2-msec execution time of the highest-priority task (calculation) is longer than the execution period required by the task that samples the gyroscope. Because the calculation task has the highest priority, no other task can pre-empt it, and the sampling task won't be able to interrupt it. Therefore, the sampling task will miss many of its deadlines while it's waiting for the calculation task to complete, and thus the calculation task will often work on inaccurate data. Consequently, this set of priorities, based solely on an intuitive understanding of the application, will drastically degrade the system's performance.

TABLE 3—RATE-MONOTONIC ALGORITHM EXAMPLE: IMPORTANCE VS PRIORITY

PERIODIC TASK	TASK IMPORTANCE (MOST = 1)	INTUITIVE TASK PRIORITY (HIGHEST = 4)	RATE-MONOLITHIC TASK PRIORITY (HIGHEST = 4)
SAMPLE GYROSCOPE	2	3	4
CALCULATE GYROSCOPE CHANGE	1	4	2
UPDATE POSITION	3	2	3
DISPLAY POSITION	4	1	1

The third column in **Table 3** shows the priority numbers that rate-monotonic scheduling assigns to the tasks. The task executed with the highest frequency, gyroscope sampling, receives the highest priority; the "most important" task (calculating the gyroscope change) gets only third highest priority. Both the sampling and position-updating tasks can pre-empt the calculations. If you wanted to implement this design with a cyclic executive, you'd have to write the calculation task as several subtasks distributed throughout the execution loop, for the same reason that the intuitively set priorities won't work. To meet the frequency requirements of the sampling task, you can't allow the calculations to take place within a single, uninterrupted block of execution time; you must break this task up manually. However, a multitasking kernel's pre-emptive tasking automatically breaks up the calculation


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Your multitasking kernel must employ a pre-emptive scheduler that allows higher-priority tasks to interrupt the execution of tasks that have lower priority.

task by letting higher-priority tasks interrupt the calculations. This example illustrates how a pre-emptive scheduler can ease the job of writing code for real-time, multitasking systems.

Split tasks to juggle priorities

If you aren't satisfied with the initial numbers you get from rate-monotonic scheduling, you can juggle task priorities to bring the system design more into line with your expectations. For example, you can break one long, infrequently executed task into two tasks, giving each of the new subtasks half the execution time of the original task. Considered as two parts of a single task, each subtask executes twice as often as the original task, and the rate-monotonic scheduling algorithm therefore assigns to each of them a priority that's higher than that of the original task.

Another approach is to write the single, large task so that it suspends its operation halfway through its work and is then restarted later by the multitasking kernel. The suspended operation of the large, high-priority task gives other tasks a chance to execute, thus preventing hard deadlines from being missed. So, if for any reason you disagree with the initial priorities that the rate-monotonic scheduling algorithm provides, you can change the way your software design works and still get equally valid numbers from the technique.

To illustrate this point, consider a system comprising a long task that absolutely must meet a hard deadline coexisting with a less critical task that executes more frequently. Normally, rate-monotonic scheduling would assign a higher priority to the less important task because of its higher execution frequency. However, you can split the more important task into two equal parts and double its frequency. The rate-monotonic scheduling algorithm now assigns a higher priority to this task than to the less critical task. During operation, the important task performs half of its duties and then terminates. The second time this task runs, it finishes the job. Whether the important task is one large task or two smaller subtasks, it does the same amount of work and uses the same amount of processor time. But by splitting up the important task, you give the less important but more frequent task a chance to run and to meet its deadlines.

The key point is that real-time systems can't tolerate long, uninterruptible tasks when other time-critical tasks need frequent service. Rate-monotonic scheduling gives you a figure of merit by which to rate your proposed software design. If rate-monotonic scheduling assigns a low priority to tasks you consider to be the most important, then your critical tasks are too big and too slow. Shorten them, rewrite them in a faster language (such as assembly code), or split them up until you meet your explicit and implicit design goals.

Finally, in addition to the rate-monotonic scheduling theory's ability to handle unsynchronized, periodic tasks, researchers at Carnegie-Mellon's Software Engineering Institute have expanded the theory to accommodate aperiodic-task processing and task synchronization. The references provide additional information on these extensions. EDN

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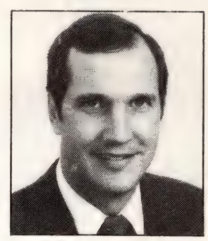

Lee Silverthorn is the president of DDC-I Inc (Phoenix, AZ). Lee has been with DDC-I for three years and is responsible for strategic planning, Ada product development, and sales/marketing. He has a BA in Math Science from Rice University, an MS in Computer Science from the University of Colorado, and an MBA from Arizona State University. In his spare time, Lee enjoys flying light planes, skiing, and photography.

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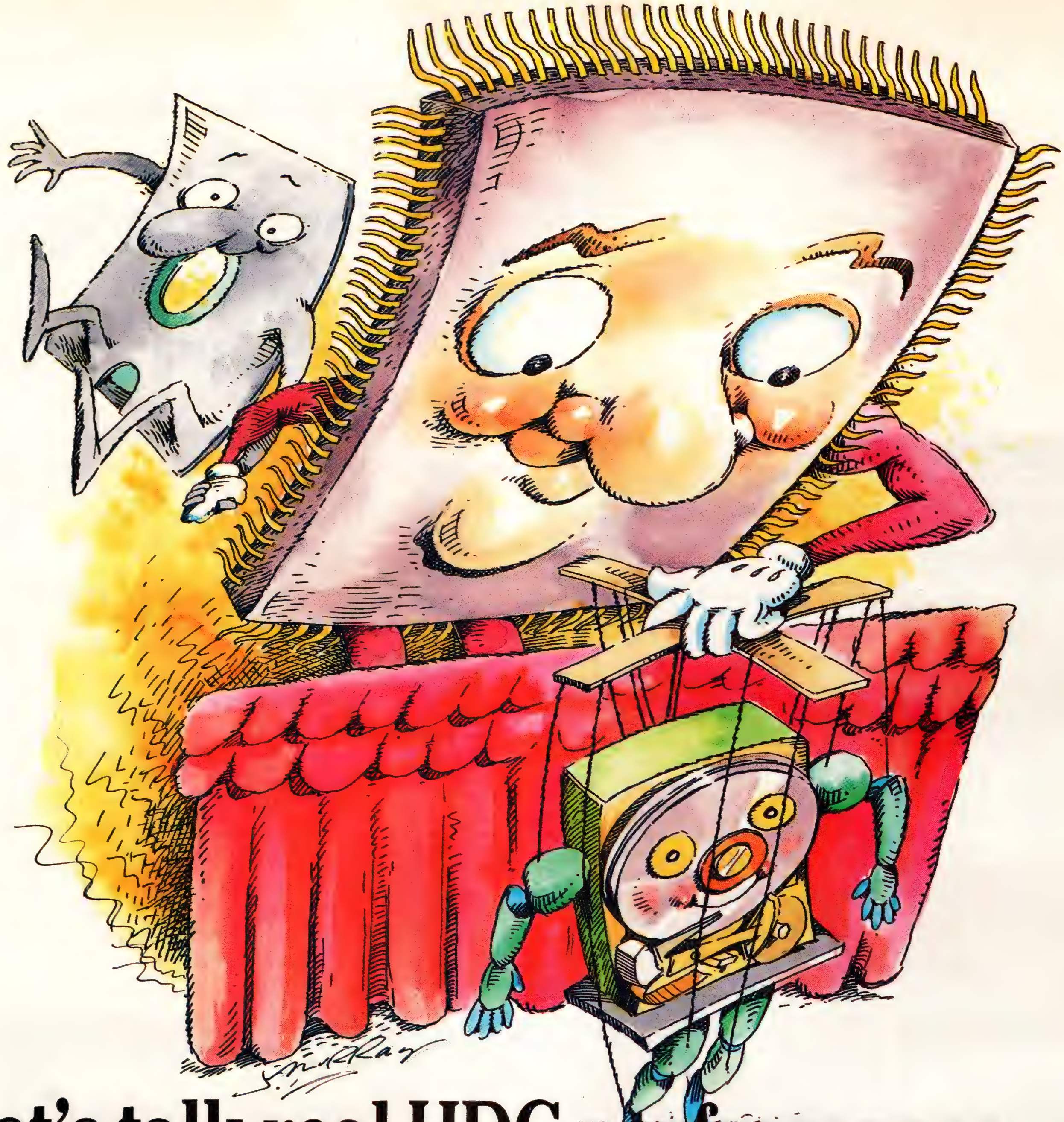

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Ease bar-code-reader design by using 8-bit A/D converters

Standard bar-code readers are expensive, but you can cut costs significantly and ease the design of these devices by combining modern A/D converters with a photodiode array.

Richard Markell, *Linear Technology Corp*

Automated pricing is a fact of life at the check-out counters in today's supermarkets; all it takes to price a product is a quick swipe across the bar-code reader. Unfortunately, low-cost, dual-slope A/D converters can't run fast enough, so today's standard bar-code readers must use expensive A/D converters. The design discussed in this article solves the cost problem and facilitates bar-code-reader design by combining a half-flash A/D converter with a 256-element, line-scan photodiode array. The system's circuitry adapts to a wide range of applications, from low-power, handheld bar-code readers to high-resolution, automated, machine-inspection applications.

The LTC1099 A/D converter in the following example features an internal sample/hold amplifier. This amplifier allows the converter to sample the individual pixels of the photodiode array at rates that maintain 8-bit accuracy to 156 kHz. This sample rate is fast enough to provide good throughput for machine-vision or bar-code scanner applications, and it doesn't require the use of an expensive flash converter.

Finding bugs in an A/D-converter-based system is never easy, and when you add a photodiode array, system-integration problems are even more difficult to locate. To simplify matters, you can employ an inexpensive, 12-bit D/A converter, configured to accept only 8 bits, as a troubleshooting aide. Once you've finalized the system design, you can remove the D/A converter.

Fig 1 shows the schematic for the system. The LTC1099 (IC_3) is configured in a write-read (WR-RD) mode. This configuration allows the system to continuously output the LTC1099's 8-bit digital data to the MP1208 D/A converter. The amplified D/A signal at the output of IC_6 represents the reconstructed digital signal—the analog signal that has been digitized and then converted back to analog by the MP1208. This output allows you to directly compare the system output to the output of the photodiode array that you're trying to digitize.

In **Fig 1,** the LTC1099 also drives the 8-bit μP bus. IC_5, a junction-FET-input op amp, converts the current output of the MP1208 to an output voltage. IC_6 amplifies and limits the bandwidth of this signal and generates a 0-to-5V output. IC_7 develops a 2.5V reference level for IC_4 and IC_3.

To illustrate A/D converter operation, **Fig 2a** shows the write-ready ($\overline{WRRDY}$) pulse from the clock circuitry (trace A) and the analog output of the photodiode array (trace B). The photodiode array outputs 256 voltage pulses; each represents the exposure of an individ-

System-integration problems are difficult to locate when you include a photodiode array in an A/D system.

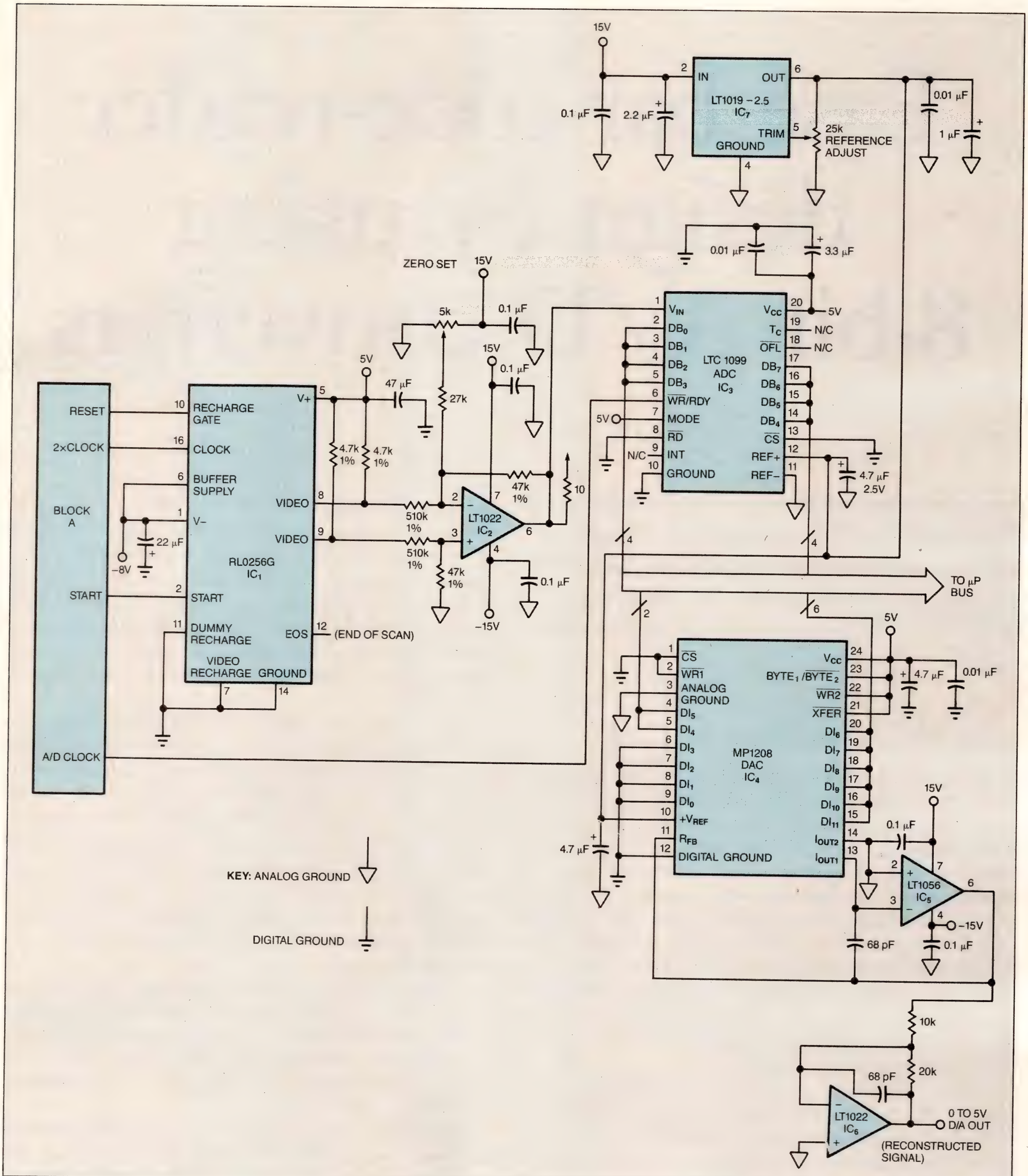

Fig 1—To simplify system troubleshooting tasks, *this optical-to-digital converter includes an inexpensive, 12-bit D/A converter (MP1208) configured to accept only 8 bits. Once you finalize the design, you can remove the MP1208.*

ual photodiode. If you could fabricate a grating that consisted of 128 black lines separated by 128 transparent spaces and then place this grating over the photodiode array, using the proper magnification, the output pulses would represent alternating full-scale and zero analog levels.

In addition, **Fig 2a** shows the analog and reconstructed digital outputs from a few pixels of the evenly illuminated array and also details the timing requirements of the LTC1099 A/D converter. The falling edge of the $\overline{WR}$/RDY pulse initiates the A/D conversion cycle. As the diagram in **Fig 2b** illustrates, the analog input must be stable 130 nsec before the negative transition of the $\overline{WR}$/RDY pulse. Approximately 110 nsec after the falling-edge transition, the internal S/H goes to the hold mode, and the analog input is ignored until the next conversion. **Fig 2a** illustrates how the circuit of **Fig 1** uses this timing cycle to sample the output of the photodiode array.

The RL0256G photodiode array shown in **Fig 1** is inexpensive, features a differential output for on-chip noise cancellation, and is simple to use (because it requires only a single-phase clock). This device contains 256 pixels; a row of silicon photodiodes, each of which have an associated storage capacitor to integrate photocurrent; and a multiplex switch for periodic readout. An integrated shift register accomplishes the readout, and a TTL clock transfers data from a row of photodiodes to the output pin. The data from a row of dummy photodiodes (photodiodes that have an opaque covering) transfers simultaneously with the data from the active photodiodes to cancel multiplex switching transients. When you use this array, you can achieve a 25-μm resolution using standard optical techniques.

Block A of **Fig 1** contains a single-phase TTL clock and associated driving signals that control the photodiode array, IC_1. The array outputs a train of 256 charge pulses for each of the video and dummy-video lines. The pulses on the dummy-video line contain only switching transients, and the pulses on the video line contain the video signal as well as the switching transients. IC_2, a FET-input op amp, operates as a differential current amplifier that outputs a pulse whose peak amplitude is scaled to a reasonable voltage level (2.5V in this case) for driving the A/D converter. A word of caution here—if IC_2 is more than three inches from the photodiode array, you should use a coaxial cable to interconnect the two circuits.

Trace D in **Fig 2a** illustrates a series of output pulses from IC_2. Sampling on the flat top of each pulse pro-

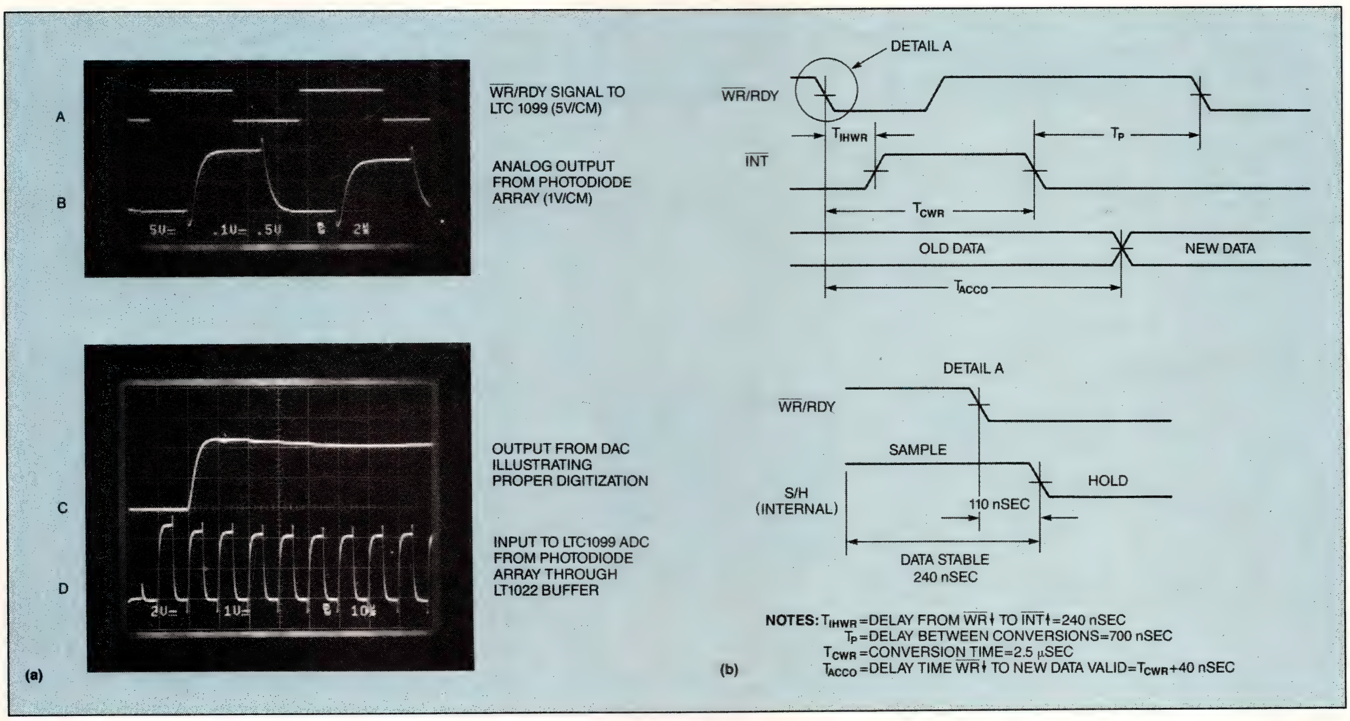

Fig 2—This detailed look at LTC1099 operation *(a) shows the $\overline{WR}$/RDY pulses from the clock circuitry (trace A), the analog output of the photodiode array (trace B), and the analog (trace D) and reconstructed digital outputs (trace C) from a few pixels of the evenly illuminated array. As the timing diagram shows (b), the analog input must be stable 130 nsec before the falling edge of the $\overline{WR}$/RDY pulse.*

It's all in the timing

Fig A details the timing circuitry of Block A in **Fig 1**. The simple TTL circuitry required to drive the array has no unusual characteristics.

IC_{10}, a crystal oscillator, supplies the clock signals. Counters IC_{13}, IC_{14}, and IC_{15}, combined with the DIP switches, set the number of clock pulses between start pulses to 4096 or any value less than that, establishing the integration time. The variable low pass at the input of three sections of IC_{12} provide a clock-delay capability to ensure that all the signals occur in the proper sequence.

A word of caution to those who might prototype this circuit: to set up the timing signals properly, you must obtain a copy of the EG&G Reticon data sheet for the RL0256G array.

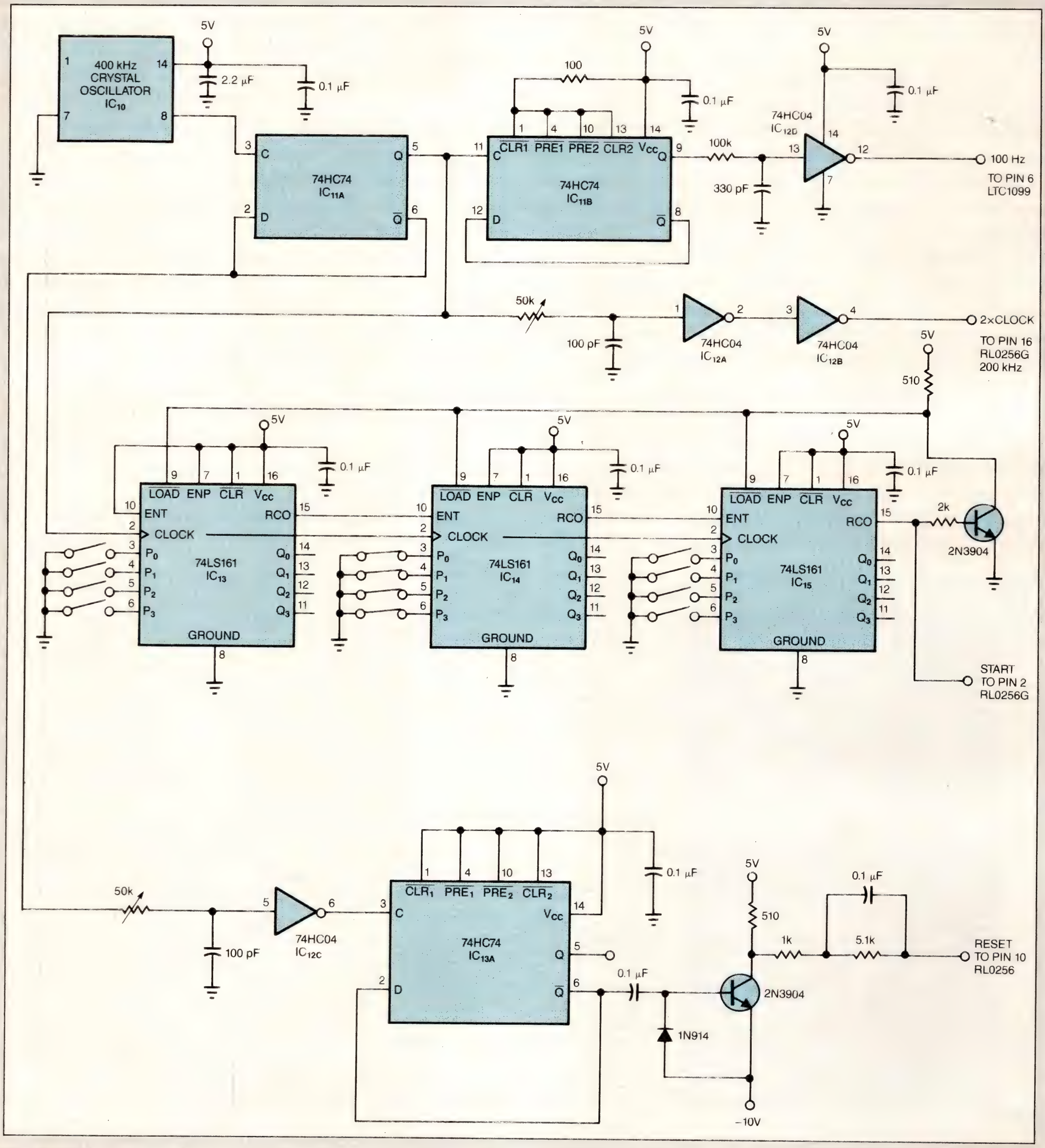

*Fig A—**Simplicity is the key feature** for the photodiode-array driving circuitry. A crystal oscillator (IC_{10}) provides the clock pulses, and the counters (IC_{13}, IC_{14}, and IC_{15}) set the number of clock pulses between start pulses.*

You'll often use baseline correction when you work with photodiode arrays.

vides an accurate analog signal for the A/D converter. Trace C in **Fig 2a** shows the test output—the reconstructed analog signal through the A/D-D/A chain. Although this output is delayed by one clock pulse, it nicely follows the signal peaks' profile of the analog photodiode pulses.

You can easily interface the A/D converter to a μP, and the converter's speed makes it easy to use baseline correction. Baseline correction, a technique in which the baseline (or dark) value of each photodiode is stored in memory, is very useful for photodiode arrays. At power-on, the dark value of each photodiode, totaling 256 individual 8-bit values, is stored in memory. This technique provides a greater dynamic range than would be available by simply using an average of all the photodiodes' dark values. The A/D converter's 156-kHz, maximum sampling rate allows a μP to perform baseline correction rapidly with little system overhead.

A look at system response

As noted earlier, the clock circuitry in block A of **Fig 1** drives the photodiode array. The D/A converter, IC_4, and op amps IC_5 and IC_6 provide a digitally reconstructed analog output, which should closely resemble the analog pulse amplitudes at the output of IC_2.

Fig 3 shows the system response when an optical grating is placed directly on the glass window that covers the photodiode array. In both scope photos, the bottom trace is the analog output from op amp IC_2, and the top trace is the output of IC_6. The line widths, which appear as notches in the traces in **Fig 3a,** measure (from left to right) 400, 350, 300, 250, and 200 μm. **Fig 3b** shows (from left to right) the system response to line widths of 200, 150, 100, 90, and 80 μm.

Designers must take the photodiode's integration time into consideration. Integration time is analogous to the shutter speed of a film camera. The longer you keep the shutter open, the more light you'll collect on the film and hence, the darker the film. The integration time for the array in **Fig 1** is approximately 6.4 msec. You can vary this parameter by varying the settings of the DIP switches connected to IC_{13}, IC_{14}, and IC_{15} (part of the circuitry in block A of **Fig 1**). In the system under discussion, keep the integration times under 40 msec at room temperature to prevent integrated dark current (leakage current in a nonilluminated photodiode) from contributing significantly to the output charge. For astronomical applications, you can cool the photodiode. Cooling decreases diode dark current and allows you to increase the integration time.

The circuit shown in **Fig 1** easily reads 80-μm line widths without having to use an optical system. Anyone with a well-designed, diffraction-limited optical system should be able to resolve 25-μm line widths without resorting to optical magnification. Of course, optical systems that utilize magnification can resolve smaller features at the expense of the field of view. The semiconductor industry, in which 1-μm line-width resolution is common, usually employs such systems.

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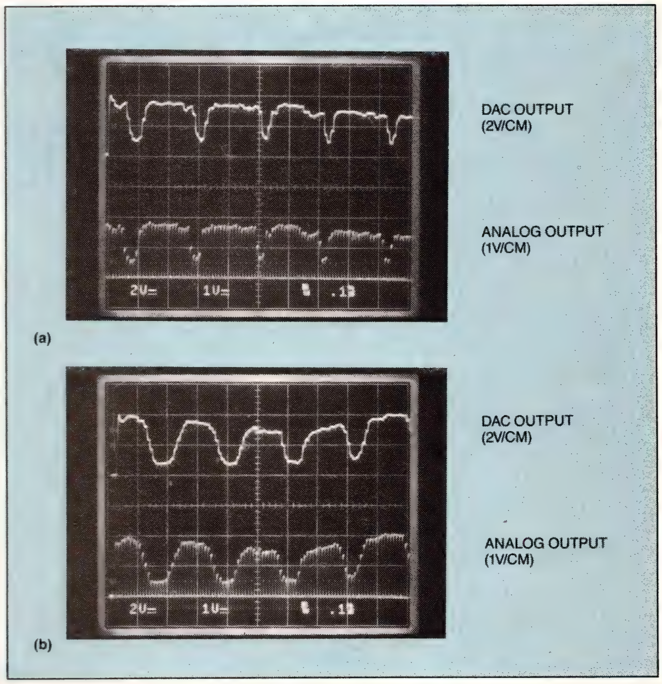
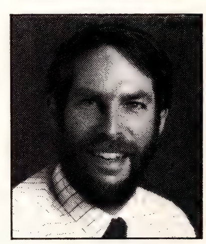


***Fig 3—System optical resolution** is determined by placing a grating directly on the photodiode array's glass window. As the bottom trace in both photos illustrates, the system readily handles (a) 400-to-200-μm or (b) 200-to-80-μm line widths.*

Author's biography



Richard Markell is the applications manager at Linear Technology Corp (Milpitas, CA). He has a BA in electro-optics from San Jose State University and has worked in the electro-optics field for Litton Applied Technology and GTE Government Systems. Before joining Linear Technology, Richard worked in analog design at EG&G Reticon and Sony Corp. His leisure interests include audio systems, gardening, cross-country skiing, and hiking.

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Current-feedback op amps extend high-frequency performance

Op amps that use current-feedback topology offer significantly higher gain-bandwidth and slew-rate performance than do conventional op-amp designs. Unique to the current-feedback design is its relatively constant bandwidth over a wide range of closed-loop gain.

James Wong, *Precision Monolithics Inc*

Compared with conventional op amps, which use voltage feedback, current-feedback amplifiers exhibit more constant bandwidth characteristics as a function of variations in closed-loop gain. Such characteristics are useful in applications such as automatic gain control, where it's desirable to preserve the useful bandwidth of the circuit as the gain varies over a wide dynamic range. You can also use these gain-bandwidth characteristics to design amplifiers that exhibit substantial gain and negligible phase error over a moderately wide bandwidth.

One example of the new generation of current-feedback op amps is the OP-260. This dual op amp has a quiescent current of 5.5 mA per amplifier. Many conventional wide-bandwidth op amps operate as high as 20 mA. The op amp's low power consumption enables encapsulation in an 8-pin mini-DIP or a small outline (SO) package.

Based on a transimpedance configuration, the OP-260 operates differently than a conventional voltage-gain amplifier. **Fig 1** illustrates the differences between the two types of op amps. A conventional op amp **(Fig 1a)** amplifies the differential voltage across the two inputs. The circuit closes the feedback loop by forcing the output signal that's fed back through R_1 and R_2 to equalize the two inputs.

Unlike the conventional op amp, whose two inputs have a high impedance, the current-feedback design **(Fig 1b)** has an input stage that consists of a unity-gain-voltage buffer amplifier. Only this noninverting input has a high impedance. The inverting input is actually a low-impedance output port, through which moderately high current can flow in or out. Following the input stage is a transimpedance stage that converts the buffer's output current to a linearly proportional output voltage.

The current-feedback loop works in the following manner: As the noninverting input voltage increases in the positive direction, the inverting input voltage follows. The buffer must source current through R_1, which causes the output voltage of the transimpedance stage to rise until its current, which feeds back to the input through R_2, equalizes the current through R_1, thus replacing the buffer's output current. Under steady-state conditions, only a minute amount of buffer-output current needs to flow in order to sustain

Current-feedback op amps are based on a transimpedance configuration that resembles a current-controlled voltage source.

an output voltage, which is determined by the divider resistors. Obviously, the ratio of $1 + (R_2/R_1)$ determines the circuit's gain—much like a conventional op amp. Similarly, in the case of an inverting amplifier, the same resistor ratio sets the gain.

Op amp is designed for a high slew rate

Fig 2 shows the basic schematic for the three-stage OP-260 op amp. A unity-gain, emitter-follower amplifier comprises the input stage. The emitters of Q_5 and Q_6 form a class AB output stage for the buffer, which can source or sink current. The buffer's output current is sensed by both the top current mirror (Q_7, Q_9, and Q_{10}) and the bottom current mirror (Q_8, Q_{11}, and Q_{12}). For example, when the buffer's output sources current to a load, current flows out of the −IN pin and Q_5's collector current increases. Thus, the buffer mirrors more current through Q_9 and Q_{15}, which increases the base drive to output transistor Q_{17}.

Conversely, increasing current in Q_9 drives Q_{13} harder, robbing base drive from the complementary output transistor (Q_{18}). This push-pull action ensures a rapid slew in the output voltage. For a small step rise, the amplifier's slew rate depends largely on the

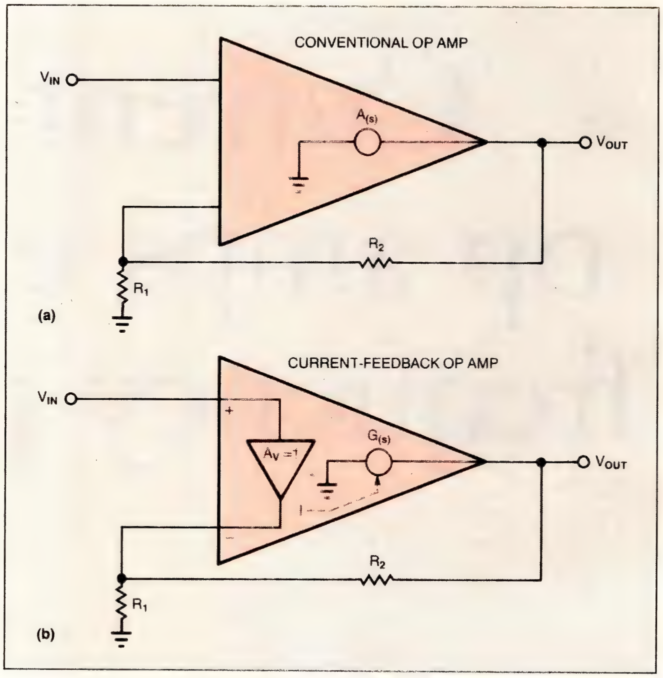

Fig 1—A conventional op amp (a) *is a voltage-controlled voltage source. By contrast, the current-feedback op amp* ***(b)*** *resembles a current-controlled voltage source.*

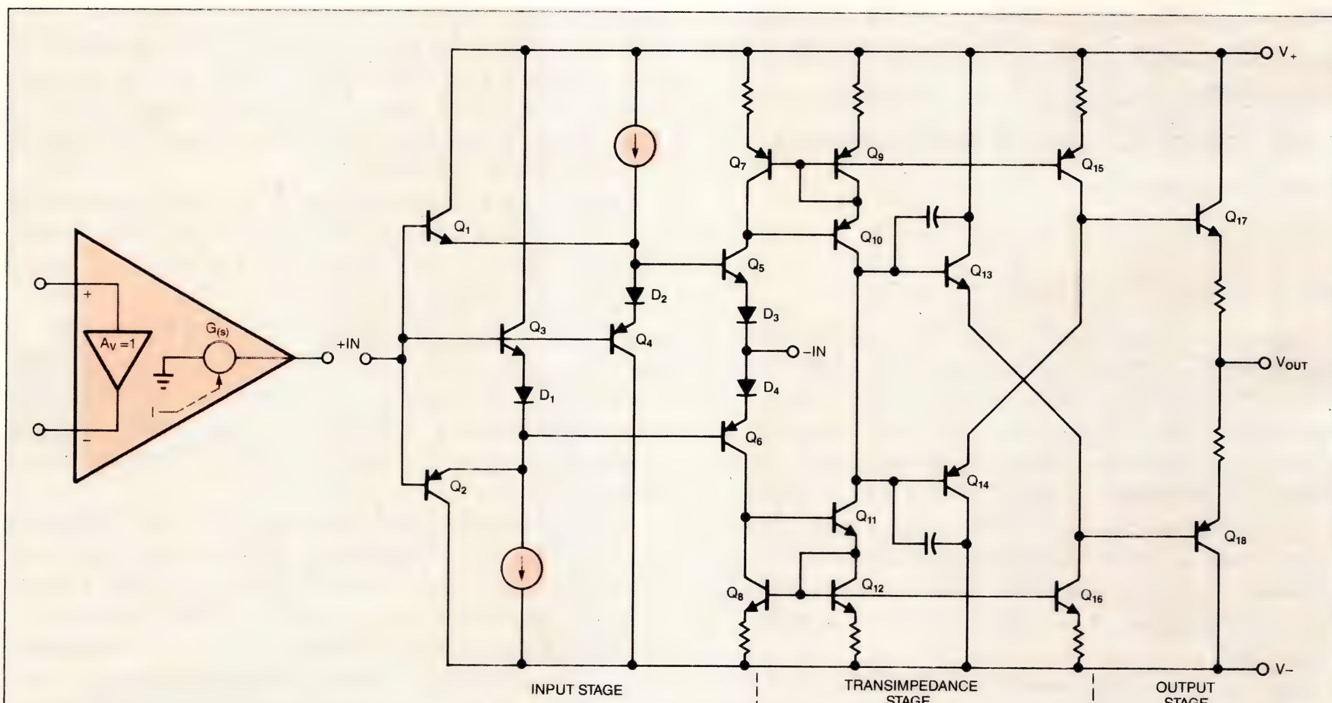

Fig 2—This simplified schematic of the OP-260 op amp *shows the input stage, the transimpedance stage, and the output stage. The equivalent block diagram is shown to the left.*

available current from the two current sources that drive the bases of Q_5 and Q_6. To increase the slew rate, especially during a large input step, Q_1 and Q_2 are added to boost the base-drive current for Q_5 and Q_6. Consequently, at a closed-loop gain less than 10, a large input step will turn on Q_1 or Q_2, thus supplying the base-drive current needed to attain a higher slew rate.

Besides using matched current sources, the OP-260 uses vertical pnp transistors instead of the more conventional lateral pnp devices. A vertical geometry extends the f_T of the pnp transistors from 2 MHz to over 120 MHz. Thus the pnp transistors' bandwidth nearly matches that of the npn transistors, resulting in an amplifier with an equivalent full-power bandwidth of over 1 MHz.

Bandwidth preservation is important

The op amp's current-feedback design ensures that its bandwidth remains relatively constant as a function of the closed-loop gain. Unlike conventional voltage-gain op amps, whose bandwidth decreases as the gain increases, a current-feedback amplifier's gain-bandwidth product increases at higher gains. **Fig 3** shows the frequency response of the OP-260 at various closed-loop gains. Note that the frequency-response curves apply for a fixed feedback resistance of 2.5 kΩ. Because the OP-260's frequency response depends primarily on the value of the feedback resistor, holding the value constant tends to hold the −3-dB frequency point within a range of closed-loop gain.

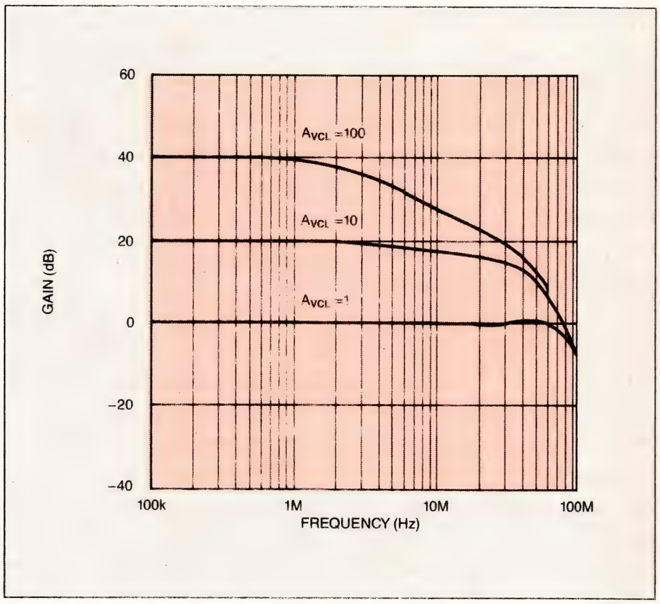

Fig 3—These curves show the frequency response *of the OP-260 when connected in three different closed-loop gain configurations. In all three cases, the circuit used a 2.5-kΩ feedback resistor and a 100Ω load. Note that the frequency roll-off curves do not follow the asymptotic roll-off characteristic of a conventional op amp.*

Using the **Fig 4** model, you can estimate the frequency response of the current-feedback amplifier. Here, the amplifier's frequency response is heavily dependent on the value of R_2. The circuit models a real but low-value output resistance (R_{INV}) at the inverting input of the amplifier (the output of the buffer amplifier). The nodal equations for V_1 and V_2 are

$$V_1 = \frac{V_{IN}(R_2/R_{INV}+V_O}{1+(R_2/R_1)+(R_2/R_{INV})}$$

$$V_2 = \frac{R_T}{1+(s \cdot R_T \cdot C_C)} I_1,$$

where

$$I_1 = \frac{V_{IN}-V_1}{R_{INV}} = V_1\left(\frac{1}{R_1}+\frac{1}{R_2}\right)-\frac{V_2}{R_2}.$$

Therefore

$$V_2 = \left[\left(\frac{V_{IN}(R_2/R_{INV})+V_O}{1+(R_2/R_1)+(R_2/R_{INV})}\right)\left(\frac{1}{R_1}+\frac{1}{R_2}\right)-\frac{V_O}{R_2}\right] \left(\frac{R_T}{1+(s \cdot R_T \cdot C_C)}\right).$$

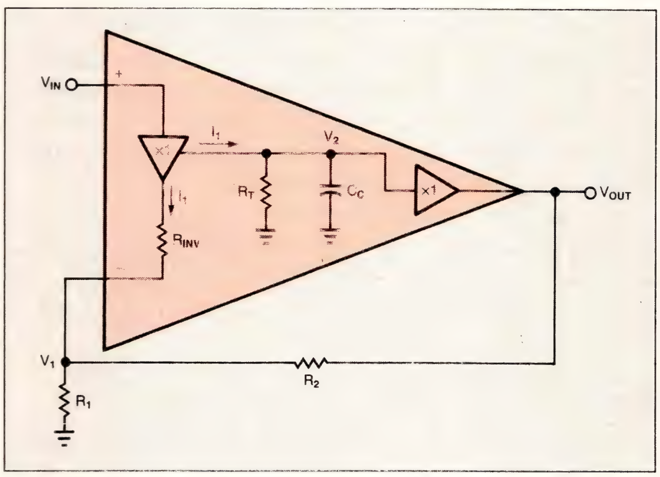

Fig 4—A simple model of a current-feedback amplifier *illustrates several important components. Shown are the small-signal transresistance (R_T), the internal compensation capacitance (C_C), the input-buffers output resistance (R_{INV}), and the feedback network (R_1 and R_2).*

A unique feature of the current-feedback design is that its bandwidth remains relatively constant as a function of the closed-loop gain.

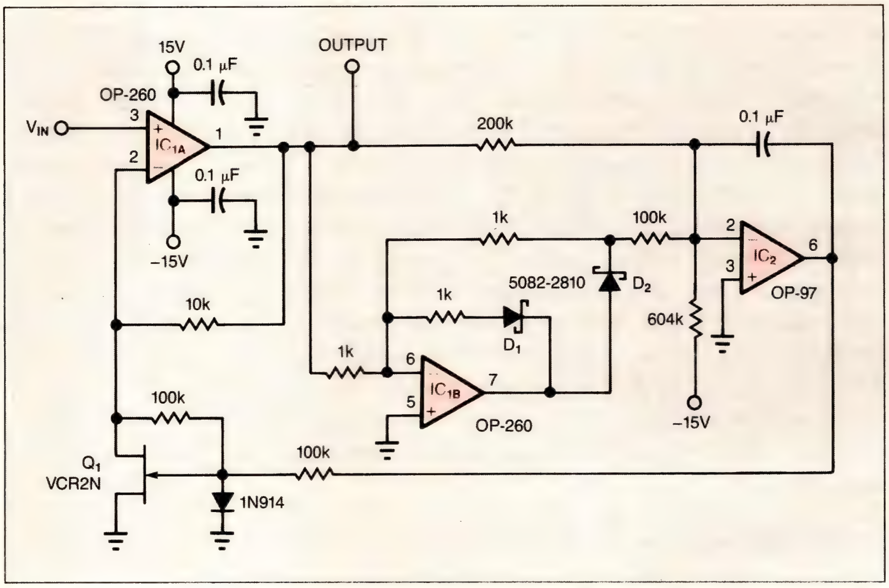

***Fig 5—AGC amplifiers** take advantage of the wide gain range of a current-feedback amplifier and its ability to preserve the circuit's bandwidth.*

If R_T is >>R_2 and R_{INV}, the transfer function simplifies to

$$\frac{V_O}{V_{IN}} \simeq \frac{1+(R_2/R_1)}{1+s[R_2+(1+R_2/R_1)R_{INV}]C_C}.$$

The importance of the last equation lies in the fact that the complex frequency variable (f_s) operates predominately on R_2. For example, at unity gain, where R_1 is infinite, R_2 determines the −3-dB frequency. Notice that as the gain increases to 10 ($1+(R_2/R_1)=10$), the −3-dB frequency is determined by R_2 plus a small value equal to R_{INV} (typically 100Ω), multiplied by the gain factor of 10. Though small, R_{INV} is not negligible, and the −3-dB bandwidth degrades approximately 30%. Nevertheless, the −3-dB bandwidth is still significantly better than that of a conventional op amp, which degrades by a factor of 10.

As the gain increases beyond a factor of 10, the multiplying effect on R_{INV} becomes increasingly dominant and, as seen in **Fig 3**, the bandwidth falls off rapidly. Again, the bandwidth is still superior to that of a conventional op amp.

Minimize stray capacitance at the input

Because of the wide bandwidth of the OP-260, parasitic input capacitance can easily destroy the amp's stability. Even though the inverting input has a very low impedance, it behaves as the summing node for the feedback. Consequently, any capacitance present at this node, whether by design or parasitic, will introduce phase lag in the circuit. As a result, the amplifier will tend to have frequency peaks, which can create overshoot and ringing when the loop is closed. Therefore, it is very important to keep the pc-board traces at the amplifier's inverting input as short as possible to avoid picking up stray capacitance.

AGC amplifier design

One of the shortcomings of using conventional op amps in an automatic-gain-control (AGC) amplifier is that its bandwidth drops off rapidly as gain increases, thus limiting the useful bandwidth of many such designs. However, by using a current-feedback op amp, you can preserve much of the available bandwidth. The simple AGC amplifier design of **Fig 5** consists of several stages. The output of amplifier IC_{1A}, which is used as the gain stage, is rectified by the second amplifier, IC_{1B}. If the output voltage swings more negative, diode D_2 becomes forward biased and D_1 becomes reverse biased, thus closing the loop on amplifier IC_{1B}. A positive voltage appears at the anode of D_2. Conversely, if the output voltage swings positive, D_2 becomes reverse biased and D_1 becomes forward biased, thus keeping the loop closed on IC_{1B}, preventing the amplifier from saturating to the negative rail. The result is an accurate positive rectification of the output signal.

The output is then compared with a reference current set up by the 604-kΩ resistor and the −15V supply. The output of the error amplifier, IC_2, drives the FET (Q_1) to whatever level is necessary to achieve a

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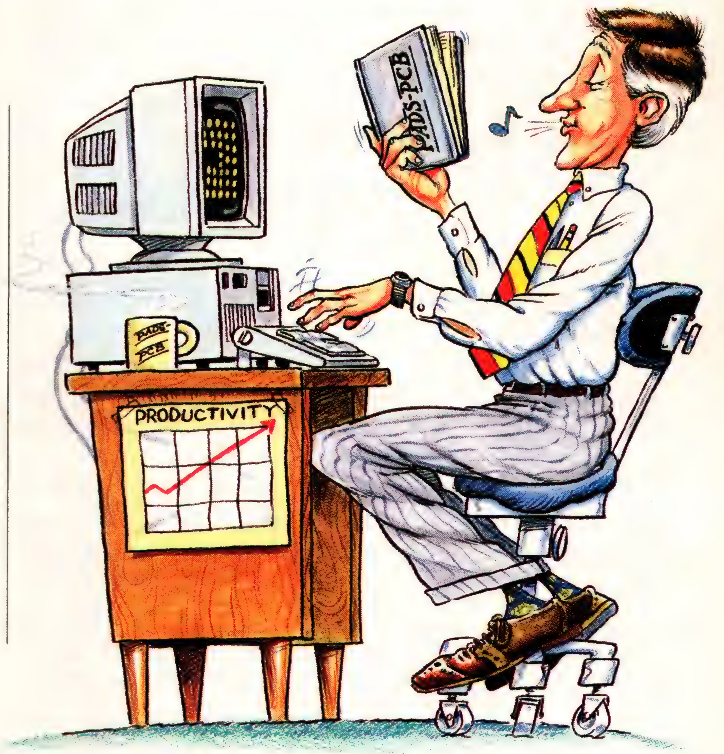

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Because of the wide bandwidth of a current-feedback op amp, you need to keep parasitic capacitances at a minimum—particularly at the inverting input.

zero voltage at IC_2's inverting input. If there is an insufficient signal, the error amplifier detects an imbalance. The imbalance causes the error amplifier to provide a more positive drive, which turns Q_1 on harder, reducing its resistance and increasing the circuit gain. These actions establish the AGC loop, which maintains a relatively constant peak-output amplitude within an input-signal range of ±20 mV p-p to ±6 V p-p.

Because the OP-260 is a dual op amp, designing an amplifier that has ultra-low phase error over a wide frequency range is significantly easier than when using single devices. The technique relies on the matched-frequency characteristics of the two monolithic amplifiers to cancel each other's poles and zeros. The circuit shown in **Fig 6** uses such a technique. Notice that the resistor-feedback networks for each amplifier are identical, and are both set for a gain of 100.

Having identical gain, the matched op amps have essentially the same frequency response. With one amplifier in the other's feedback loop, a pole in the feedback becomes a zero. And, because the pole and the zero are at the same frequency, they cancel each other exactly. The result is exceptionally low phase error. Notice in **Fig 7** that at a gain of 100, the low-phase-error amplifier exhibits less than 1° of phase shift over a frequency range that extends to over 1 MHz. Such performance is equivalent to a conventional amplifier with a gain-bandwidth product of more than 1 GHz.

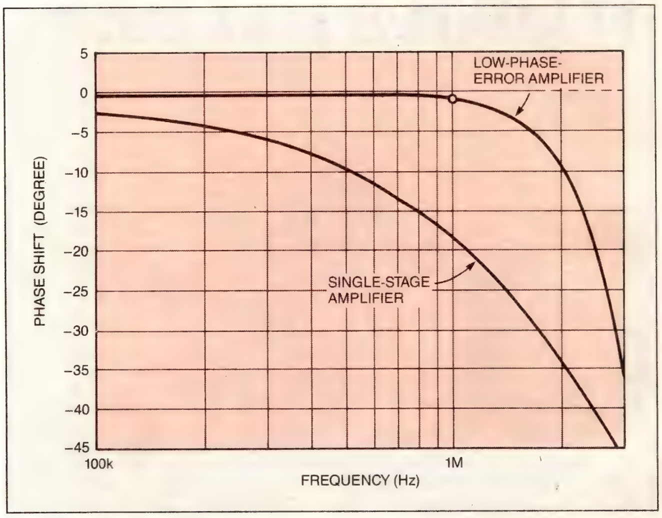


***Fig 7—This plot shows the phase response** of the low-phase-error amplifier of **Fig 8** compared to that of a single amplifier. Note that there is less than 1° of phase error over a 1-MHz bandwidth.*

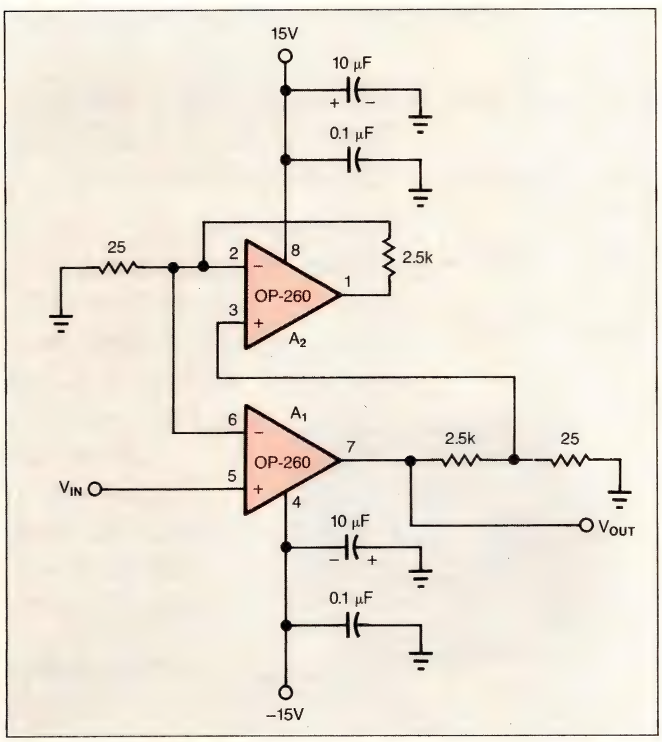


***Fig 6—An active-feedback circuit** provides cancellation of the dominant poles, which significantly reduces the circuit's phase shift.*

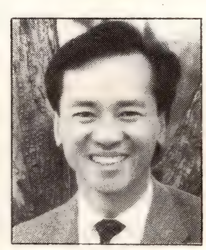
The capability that current-feedback op amps offer for high-speed performance holds great promise for many applications which, heretofore, were restricted to less cost-effective designs. EDN

References

1. *1988 PMI Data Book*
2. Wong, J, "Active feedback improves amplifier phase accuracy," *EDN*, September 17, 1987.
3. Soliman, Ahmed M, "Design of high-frequency amplifiers," *IEEE Circuits and Systems*, June 1983.

Author's biography

James Wong is manager of applications engineering at Precision Monolithics Inc. His duties include designing analog circuits, publishing application notes and articles, and developing technical seminars. James has a BSEE from San Jose State University and an MBA from the University of Santa Clara. His hobbies include golf, reading, and business ventures.



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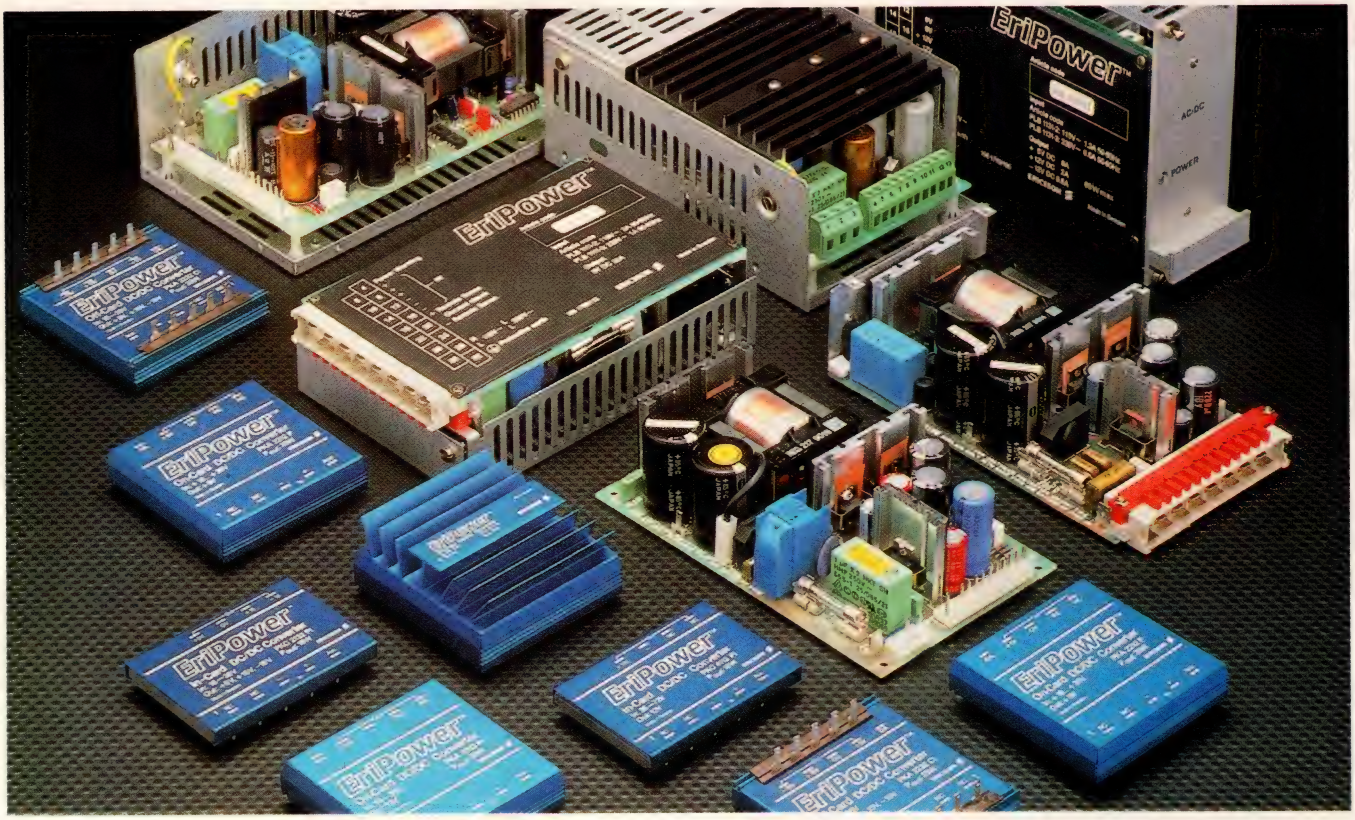

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DESIGN NOTES

Number 27 in a series from Linear Technology Corporation October, 1989

Design Considerations for RS-232 Interfaces

Sean Gold

Introduction

When designing an RS-232 interface, it is necessary to conform to standards published by the Electronics Industry Association, EIA RS-232.V28. Some key specifications are summarized in Table 1. However, the EIA specifications are often just the beginning of the design. Practical problems such as generating RS-232 signal levels, providing sufficient load drive, and ensuring protection against fault conditions must also be considered.

Table 1. Key RS-232 Transceiver Specifications (EIA RS232C.V28)

SPECIFICATION	VALUE	UNITS
Signal Levels	± 15 Max; ± 5 Min	V
Cable Length	50 Max	Ft
Load Capacitance	2500 Max	pF
Cable Termination	3k < R < 7k	Ω
Data Rate	20k Max	Baud
Slew Rate	3 < SR < 30	V/µs
Fault Conditions	Drivers Must Tolerate:	
	* Conductor to Conductor Shorts	—
	* Line Open Circuit	—
	* ± 25V Line Overvoltage	—

Power Supply Generators

Creating the separate RS-232 voltage levels is a common problem in systems which have only a 5V logic supply. Linear Technology has developed a family of transceivers that include an on-chip charge pump to generate the RS-232 supplies. These transceivers are available in a wide variety of configurations incorporating up to 5 drivers and 5 receivers. Some transceivers have a SHUTDOWN control which turns off the charge pump and places the drivers in a "zero" power—high impedance state.

The charge pump consists of a relaxation oscillator, a capacitive voltage doubler, and a capacitive voltage inverter. The oscillator is designed to operate at a frequency well above the signal frequencies to avoid supply degradation as charge is rapidly removed from the storage capacitors.

The LT1180/LT1181's charge pump oscillator operates at approximately 200kHz, which is two times the frequency of the LT1080 and LT1130 series transceivers. The faster oscillator permits the use of low value capacitors ($C > 0.1\mu F$), and shortens the turn-on time from power off or SHUTDOWN state to less than 200µs. The LT1080 and LT1130 start up in approximately 2ms.

Load Driving

It is often desirable to exceed the 20kHz data rate or drive loads greater than 2500pF, e.g. long cables. Slew rate control in the drivers makes this objective possible without compromising the remaining specifications. When lightly loaded, the slew rate is set by an internal bias current and compensation capacitor. When heavily loaded, slew rate is limited by the output stage short circuit current and the load capacitance. The plot in Figure 1 shows the maximum load capacitance for a given data rate.

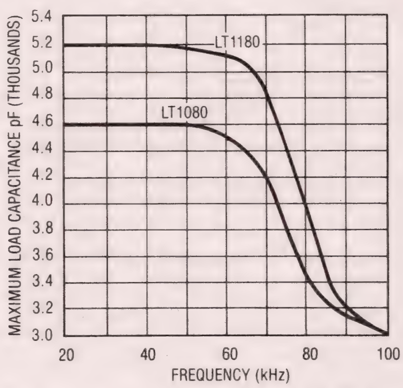
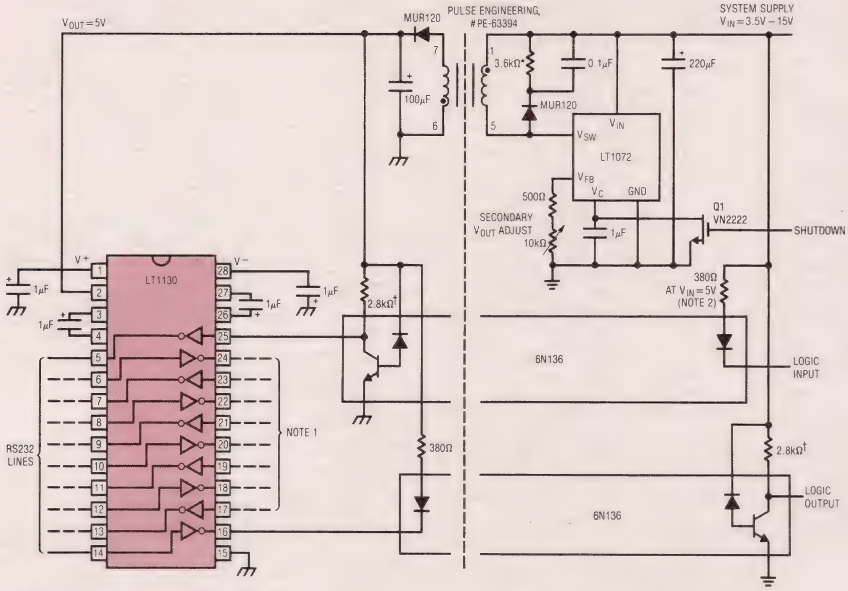


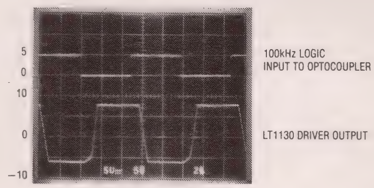
Figure 1. Max Load Capacitance vs Data Rate. Both Transceivers Use 1.0µF Storage Capacitors.



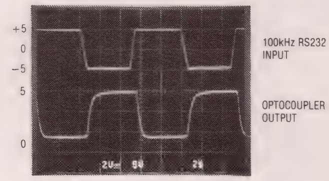
= SYSTEM GROUND

= FLOATING COMMON

NOTE 1: REPEAT THE OPTOCOUPLER CONNECTIONS FOR EACH LINE.
NOTE 2: SELECT FOR 10mA THROUGH LED
*FOR IMPROVED EFFICIENCY, REPLACE THE 3.6kΩ RESISTOR WITH A 30V ZENER DIODE
†INCREASE COLLECTOR RESISTANCE WHEN USING OPTOCOUPLERS WITH LOWER CURRENT TRANSFER RATIO.



RS232 Driver Signals



RS232 Receiver Signals

Figure 2. 2500V Isolated 5-Driver/5-Receiver RS232 Transceiver

Fault Conditions

In addition to protecting against all of the fault conditions described in Table 1, LTC transceivers are guaranteed for latchup free operation. When the drivers are turned off or SHUTDOWN, the output stage becomes a high impedance; even when the output is pulled beyond the supply rails. The small current produced by overvoltage is not directed back into the supplies. High impedance on the driver outputs also eliminates signal feedthrough between the logic inputs and the RS-232 lines.

When the device is turned on, overvoltage can, at most, pull the limited short circuit current from the supplies. The receivers are also short circuit current limited to prevent damage to unprotected logic circuitry.

Isolated Transceiver

The most frequent cause of failure in interface chips is exposure to extreme fault conditions. Protection against large differences in ground potential, high ground loop currents, or accidental high voltage connections mandates a fully isolated transceiver.

The circuit in Figure 2 provides 2500V isolation with optically coupled data lines and an isolated 5V supply. A powered transceiver eliminates the need for three supplies on both sides of the isolation transformer. High speed 6N136 optocouplers permit the LT1130 to operate at its full 100kHz bandwidth. However, slower, less expensive optoisolators, such as the 4N28, may be used when the data rate is less than 20k baud. The 5V power supply is generated with an isolated LT1072 switching regulator. The LT1072 has no electrical connection to the load; instead, the circuit derives its feedback from the transformers flyback voltage. This technique is often referred to as an isolated flyback regulator[1]. The regulator needs to deliver only modest current levels (200mA max), allowing a physically small isolation transformer. The circuit accepts 3.5V to 15V unregulated inputs which are readily available in most systems. Load regulation is 5% over a 200mA range of output current (50mA-250mA), and efficiency reaches 60% under maximum load conditions. Efficiency may be improved by 10% if the 3.6kΩ snubber resistor is replaced with a 30V Zener diode. Q1 provides shutdown control, which disables the interface to a low power state.

Note 1: Refer to Linear Technology's Application Note 19, pp. 30–34.

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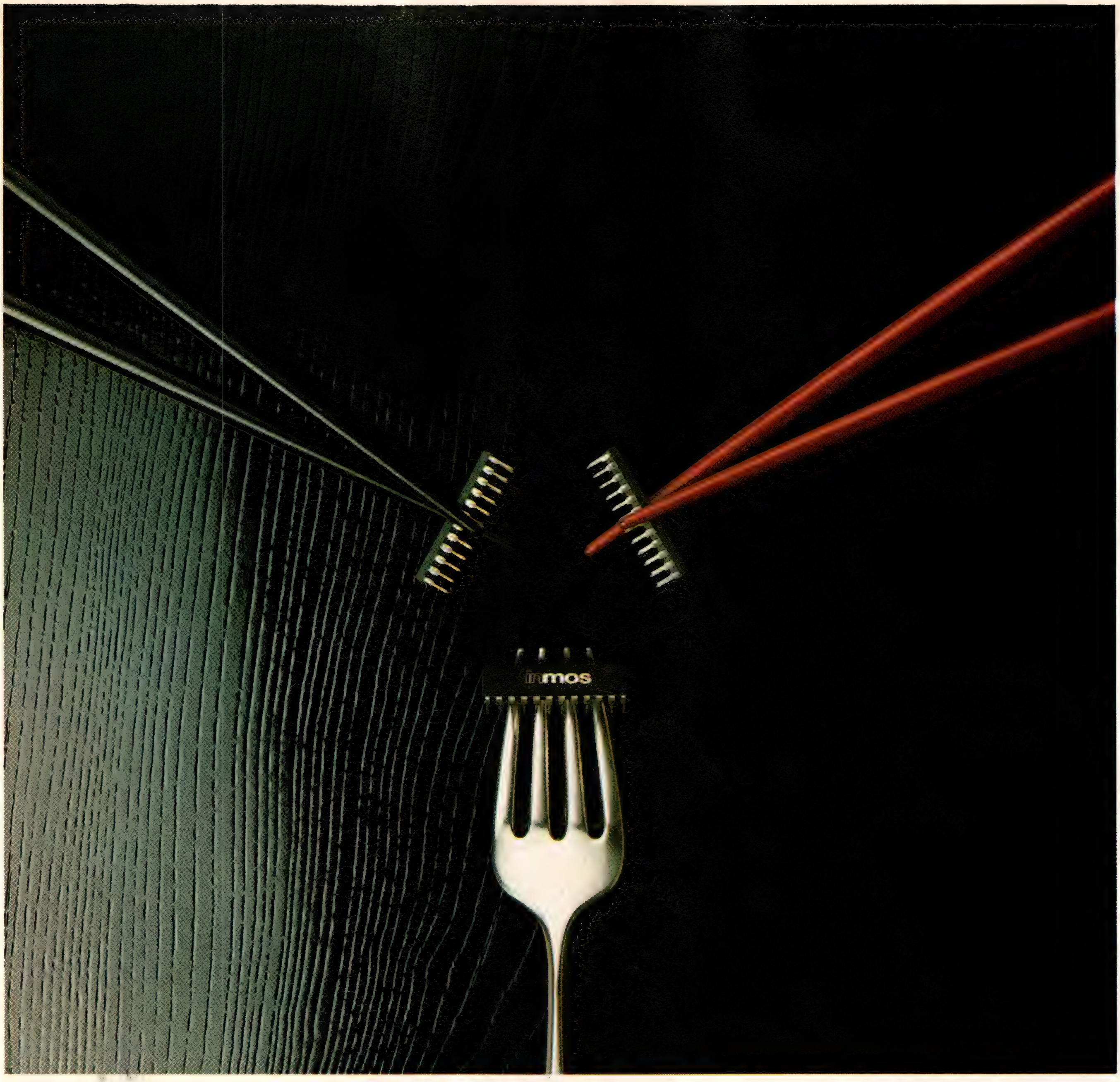
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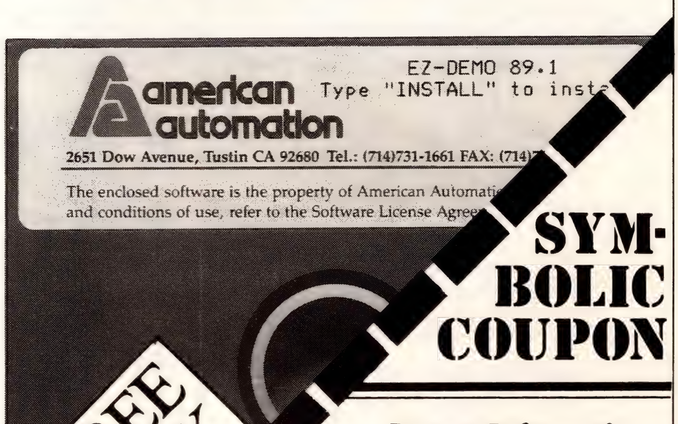

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DSP-μP routine computes magnitude

Amarnath Palacherla
Microchip Technology, Chandler, AZ

The 320C10 DSP μP program in **Listing 1** computes the magnitude of a complex number, X+jY. Finding the sum of the squares of the real (X) and imaginary (Y) parts of a complex number is no problem with a 320C10 because the IC performs a multiplication in one instruction cycle (122 nsec at 32.8 MHz).

But finding the square root of the sum of the squares is not trivial. If you use common iterative methods, such as the Newton-Raphson method, the 320C10 will take 350 or more clock cycles for this calculation (42 μsec).

The method embodied in the **listing** takes only about 30 clock cycles (3.7 μsec) and uses the following approximation:

$$Z = \sqrt{(X^2 + Y^2)} \approx \text{MAX}(X,Y) + K*\text{MIN}(X,Y).$$

The MAX(X,Y) function examines the real and imaginary parts of a complex number and selects the part having the largest *absolute* value. MIN(X,Y) similarly looks for the absolute minimum part of each complex number in your sample set. You can choose any value for the constant K between 0.25 and 0.31. Recommended values for K are 0.267304 for exact extimated mean, and 0.300585 for minimum variance.

Fig 1 graphs the percentage error between the actual value of the complex number's magnitude and the algorithm's estimate for phase angles in the first octant. Note that the maximum error is about 11% for K=0.267304, but the mean error is 0. The second routine in **Listing 1** modifies the algorithm slightly to lessen the estimate's error for phase angles greater than 41°. In pseudocode, the modified algorithm is

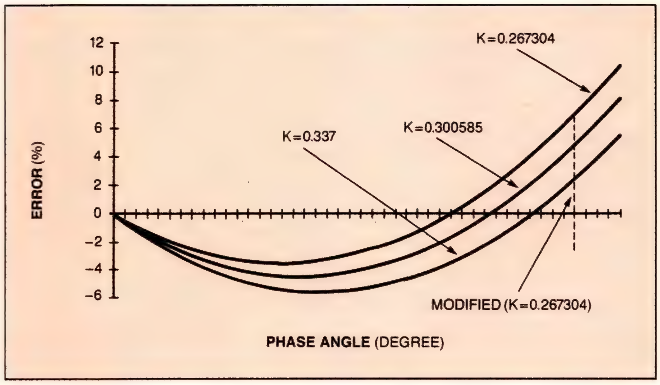

***Fig 1—This plot graphs the percentage** error between the actual magnitude of a complex number and the approximating algorithm's estimate of the magnitude against the phase angle of the complex number over just the first octant. The graph does not show that for K=0.2867304, the mean error equals zero.*

```
x1 = MAX [ ABS(x), ABS(y) ] ;
y1 = MIN [ ABS(x), ABS(y) ] ;
IF ( x1 == y1 ) THEN Z = SQRT(2)*x1 ; RETURN ;
z = x1 + K*y1 ;
IF [ y1 > x1*TAN(41) ] THEN z = z * 1.09865; RETURN ;
```

This algorithm yields a maximum error of less than 6%. Of course, with this modification, the mean error is no longer zero. EDN

References

1. Onoe, Morio, "Fast Amplitude Approximation Yielding Either Exact Mean or Minimum Deviation for Quatrature Pairs," Proceedings of the IEEE, July 1972.

2. Knuth, D E, *The Art Of Computer Programming: Volume II*, Addison-Wesley Publishing Co, Reading, MA.

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LISTING 1—COMPLEX-NUMBER MAGNITUDE ROUTINE

```
*****************************************************
*         Compute Magnitude , Z = SQRT( X*X + Y*Y )     *
*****************************************************
*         Assume X & Y are in Locations 0 & 1 Respectively
*
x         equ      0
y         equ      1
max       equ      2
min       equ      3
z         equ      4
```

LISTING 1—COMPLEX-NUMBER MAGNITUDE ROUTINE—continued

```
K       equ     5
theta   equ     6

const   DATA    8759            /***  0.267304*32768  ***/
angle   DATA    -28485          /*** -Tan(41)*32768    ***/
root2   DATA    13573           /***  sqrt(2)-1  **/

mag     lac     y
        abs
        sacl    min
        lac     x
        abs
        sacl    max
        sub     min
        bz      case1
        bgez    comp
        lar     AR0,max
        lac     min
        sacl    max            /***   max =  y  ***/
        sar     AR0,min        /***   min =  x  ***/
comp    lack    const
        tblr    K              /*** Load Constant K from ROM
***/
        lac     max,15
        lt      K
        mpy     min
        apac
        sach    z,1
**********************************************************
*         This Part of Code Necessary only if            *
*               Modified Method is Used                  *
**********************************************************
        lack    angle
        tblr    theta
        lac     min,15
        lt      theta
        mpy     max
        apac
        bgez     case2         /** branch if min > max*Tan(41)
***/
        ret
case2   lac     z,15
        lt      z
        mpyk    3233
        apac                   /** z = z*1.0985 ***/
        sach    z,1
        ret
case1   lack    root2         /**  if ( x == y ) z = x*1.414
**/
        tblr    min
        lt      min
        mpy     max
        lac     max,15
        apac
        sach    z,1
        ret
```

C program rotates vectors

Branko Zebec
PEL Electronics, Varazdin, Yugoslavia

The C program in **Listing 1** rotates a vector through an arbitrary angle quickly because it substitutes division-by-2, addition, and subtraction for the usual trigonometric calculations. The program rotates a vector and displays each increment of rotation on an IBM PC's screen (CGA card required).

Fig 1 shows a vector, r, being rotated through an angle, α. If the coordinates of the vector's endpoints are (x,y), then the coordinates of the rotated vector's endpoints, (x′,y′), are

$$x' = x\cos\alpha - y\sin\alpha$$
$$y' = x\sin\alpha + y\cos\alpha.$$

To understand how you can avoid using sine and cosine functions to perform these calculations, first recall that for very small angles sineα≈α. Then consider that for any angle α between 0 and 1 radians (0° and 180°), you can find an integer, n, which relates the angle to a power of 2:

$$\alpha = \frac{1}{2^n}.$$

Next, factor in the elementary trigonometric identities:

$$\sin^2\alpha + \cos^2\alpha = 1$$
$$\cos\alpha = (1 - \sin^2\alpha)^{1/2}$$
$$\cos\alpha = \left(1 - \frac{1}{2^{2n}}\right)^{1/2}.$$

Further, you can expand the previous equations into the Taylor series for $(1-x)^{1/2}$. Using only the first two terms in the series, you arrive at the following approximation for the cosα, which involves no trigonometric math—just calculations that suit computers:

$$\cos\alpha \approx 1 - \frac{1}{2\times 2^{2n}}.$$

Going back to the original rotation equations and substituting these last approximations yields

$$x' = x - \frac{x}{2\times 2^{2n}} - \frac{y}{2^n}$$
$$y' = y - \frac{y}{2\times 2^{2n}} + \frac{x}{2^n}.$$

Finally, to rework these expressions into forms you can program in C, make the following substitutions:

$$x1 = x/2^n$$
$$x2 = x1/(2\times 2^n)$$
$$y1 = y/2^n$$
$$y^2 = y1/(2\times 2^n),$$

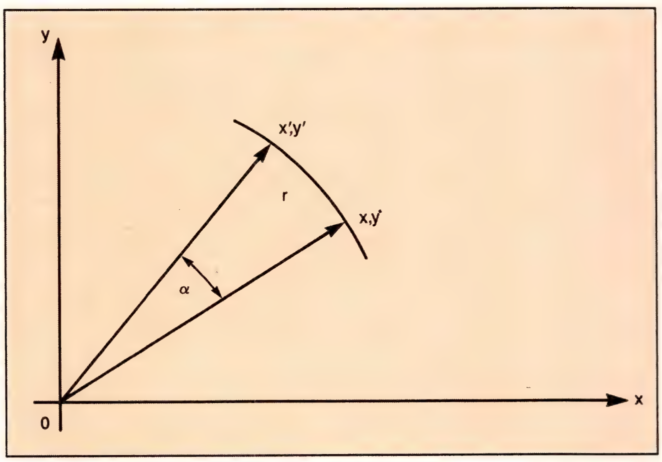


Fig 1—Rotating a vector involves translating its endpoint from one set of coordinates to another.

LISTING 1—FAST-ROTATION PROGRAM IN C

```
#include <stdio.h>
#include <dos.h>
                          /************************************************/
#define START 22600       /* must be large enough against int. underflow */
#define IMAX  50          /* IMAX * alpha = 360 [deg]                    */
#define XC    320         /* screen center ...                           */
#define YC    100         /* ... for CGA graphics card                   */
                          /************************************************/

rotate()  /* compute and plot */
{
  int x, y, x1, x2, y1, y2, i;
```

LISTING 1—FAST-ROTATION PROGRAM IN C—continued

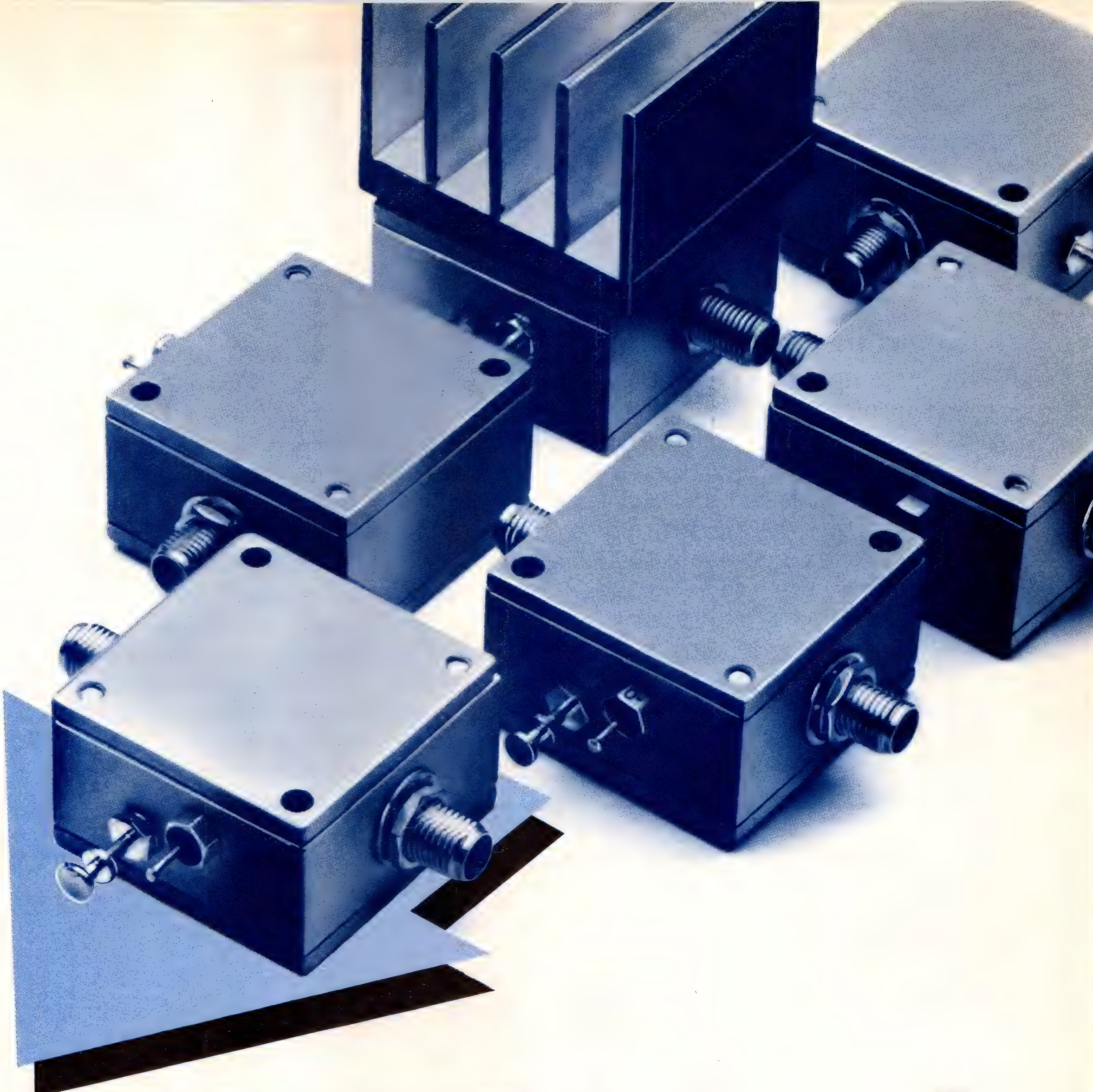
```
    x = y = START;   /* alfa start = 45 [deg] */
    for ( i = 0; i < IMAX; i++ ) {
      x1 = (x >> 3);
      x2 = (x1 >> 4);
      y1 = (y >> 3);
      y2 = (y1 >> 4);
      x = x - x2 - y1;
      y = x1 + y - y2;
      plot((x >> 8) + XC, (y >> 9) + YC, 1);  /* scaled plot */
    }
}

setgr()  /* set graphic mode - BIOS */
{
  union REGS inreg, outreg;

  inreg.h.ah = 0;
  inreg.h.al = 6;   /* 640 x 200 B/W */
  int86(0x10, &inreg, &outreg);
}

settxt()  /* set text mode - BIOS */
{
  union REGS inreg, outreg;

  inreg.h.ah = 0;
  inreg.h.al = 3;
  int86(0x10, &inreg, &outreg);
}
plot(x, y, mode)  /* set point - BIOS */
int x, y, mode;
{
  union REGS inreg, outreg;

  inreg.h.ah = 0x0c;
  inreg.x.cx = x;
  inreg.x.dx = y;
  inreg.h.al = mode;
  int86(0x10, &inreg, &outreg);
}

main()
{
  setgr();
  printf("Press any key for start ...");
  getch();
  rotate();
  printf("Press any key for exit ...");
  getch();
  settxt();
}
```

which lead to the following operations using the C operators for shifting, addition, and subtraction:

```
x1 = x >> n;
x2 = x1 >> (n + 1);
y1 = y >> n;
y2 = y1 >> (n + 1);
x = x − x2 − y1;
y = y − y2 + x1;
```

The program in the **listing** uses a value of 3 for n, which translates to angular displacements of one-eighth of a radian (7.162°). You can substitute other values for n to rotate your vectors by different increments. EDN

To Vote For This Design, Circle No 749



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ZFL-500LN	0.1-500	24	+5	2.9	79.95
ZFL-750	0.2-750	18	+9	6.0	74.95
ZFL-1000	0.1-1000	17	+9	6.0	79.95
ZFL-1000G*	10-1000	17	+3	12.0	199.00
ZFL-1000GH*	10-1200	24	+9	15.0	219.00
ZFL-1000H	10-1000	28	+20	5.0	219.00
ZFL-500HLN	10-500	19	+16	3.8	99.95
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95
ZFL-1000VH	10-1000	20	+26	4.5	229.00
ZFL-2000	10-2000	20	+17**	7.0	219.00

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CIRCLE NO 183

FEEDBACK AND AMPLIFICATION

String routine harbors bug

The routine described in the Design Idea "C string comparer handles abbreviations" (EDN, April 13, 1989, pg 214), could be very useful. However, it contains a minor bug that would allow bogus short forms for common command strings. For example, it would allow WW or even WOOOOOOO as equivalents of WordDump. This bug would make finding a distinction between WordDump and WordWrite impossible, for example.

Not incrementing both string pointers whenever a character match occurs causes the bug. I have rewritten the function in ANSI-standard C in the accompanying **listing**. This version is certainly more terse than the original and therefore less easily understood (C programmers like it that way) but is slightly more efficient. Incrementing both pointers after an initial match initializes the "for" loop. Iterations of the "for" loop occur, therefore, only upon a match. Consequently, this version does not have the bug of the original because the pointers are incremented on subsequent iterations as well as on the first iteration.

I believe the name "stracmp" for "string abbreviation compare" more accurately describes the function and also follows the ANSI-standard naming convention for string-handling routines.

Les Aldridge, President
Aldridge Real-Time Software Inc
38 Janet Ct
Milltown, NJ 08850

LISTING 1—REVISED STRING-MATCHING ROUTINE

```
#include <ctype.h>

int stracmp(char *pat, char *abbr)
{
/*
     Abreviation handling string compare. The abbr string is
     considered a match with the pattern if every character
     in abbr is matched with a character in pat. However,
     abbr need not contain every character of pat.
     This version
        1. Avoids the problem of matching
             WW,WOOOO,WDD,etc. with WordDump
        2. Improves efficiency slightly.
        3. Uses ANSI standard C structure and is named
           similarly to other ANSI standard string
           procedures,
             e.g. stricmp, strncmp.
*/
    if (toupper(*pat) != toupper(*abbr)) return(-1);

    for (abbr++,pat++; *abbr; abbr++,pat++)
        while (toupper(*pat) != toupper(*abbr))
            if (*pat++ == 0) return(-1);
    /* success */
    return(0);
}
```

FEEDBACK AND AMPLIFICATION

Single cell lights LED

The circuit in **Fig 1** improves on the design presented in "Single cell lights LED" (EDN, April 27, 1989, pg 220). In comparison with the earlier circuit, this circuit is simpler, more stable, and allows you to easily change the LED's intensity.

The 74HC14 hex Schmitt trigger works at a very low voltage. In the circuit, IC_{1A} and its resistor and capacitor form an RC oscillator, which runs at a few kilohertz. The other inverters are paralleled to increase the circuit's power-handling capability. When the paralleled inverters' outputs are low, current flows through the inductor. When the inverters go high and interrupt, current flows through the inductor, and the flyback voltage of the inductor lights the LED. The LED clamps the flyback voltage to a safe level for the IC. Because of the circuit's operating frequency, the series inductor, L, has a high impedance. Therefore, you do not have to worry about overcurrents damaging the IC.

You can reduce current draw and dim the LED if you disconnect one or more of the paralleled inverters.

Yongping Xia, Research Assistant
Electrical and Computer Engineering
817 Engineering Science Bldg
Morgantown, WV 26506

(Ed Note: *Readers also might consider the LM3909 LED-flasher IC. This 12-year-old part uses a capacitive voltage doubler to power a flashing LED from a single cell.)*

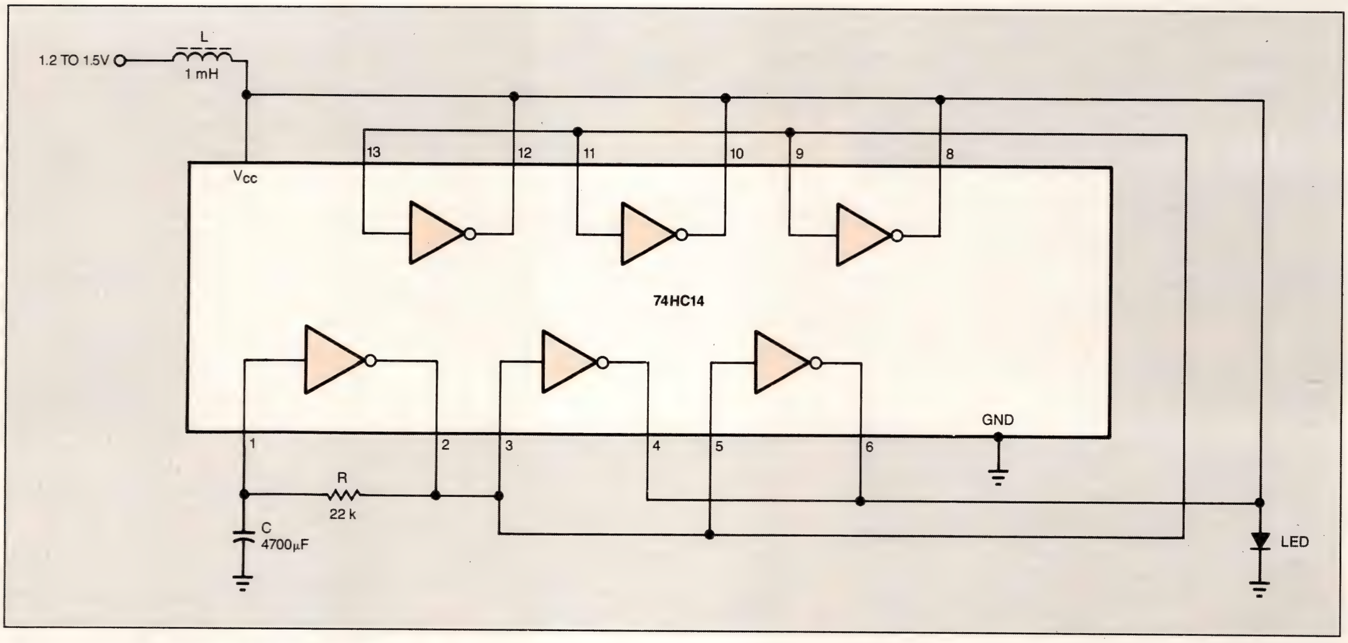

Fig 1—A single cell can light *an LED with this circuit.*

Author relates positive feedback

The Design Ideas editor of EDN put me in touch with a reader who had a problem with my Design Idea, "Program calculates BPF component values" (EDN, May 11, 1989, pg 200). (Ed Note: BPF means bandpass filter.) After we found that he had made an incorrect entry, he was able to run my program successfully.

I have had over a dozen personal phone calls (even two at home) on the time savings that engineers have realized by using my program. A recent conversation with a design engineer in Tennessee resulted in some useful improvements to my program.

I want to thank you for the opportunity to write for EDN. And, in the future, I look forward to submitting other design ideas.

Bob Mostafapour, Design Engineer
Dow Corning Corp
Midland, MI 48640

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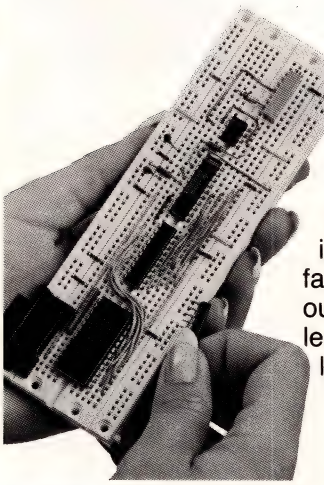

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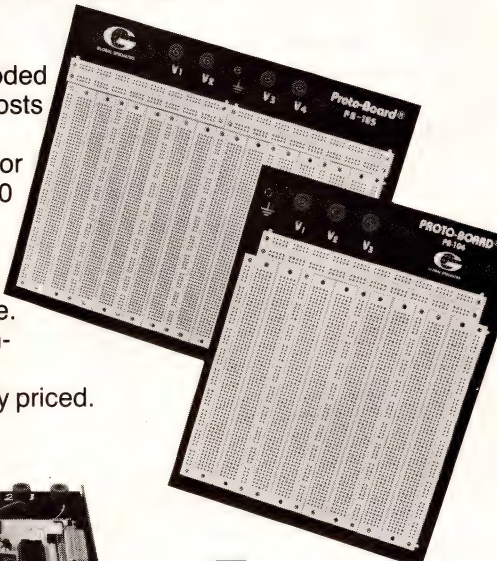

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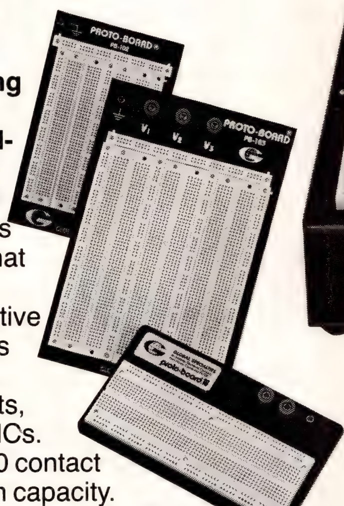

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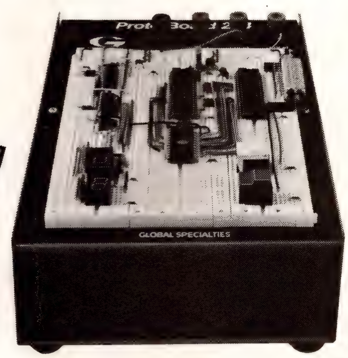

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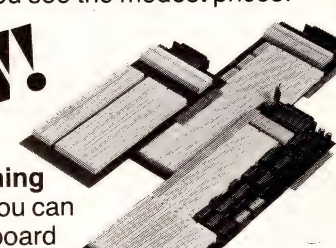

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CIRCLE NO 185

A0011

Design Entry Blank

$100 Cash Award for all entries selected by editors. An additional $100 Cash Award for the winning design of each issue, determined by vote of readers. Additional $1500 Cash Award for annual Grand Prize Design, selected among biweekly winners by vote of editors.

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ISSUE WINNER

The winning Design Idea for the August 3, 1989, issue is entitled "Generator rumbles at low frequencies," submitted by Andrew Dart of Andy's Bureau of Standards (Duncanville, TX).

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CIRCLE NO 188

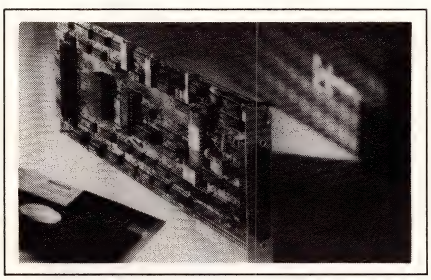
DEVELOPMENT SYSTEM

- *Offers logic analyzer, ICE, and PROM/PLD programmer*
- *Supports 68000, 8086, Z80, and others*

The FDS-128 combines a zero-wait-state in-circuit emulator, a 40-channel, 40-MHz logic analyzer, and an EPROM/PLD programmer. The unit supports widely used μPs, including the 68000, 8086, 8088, Z80, 6502, and 6802. The instrument can stand alone—it has a 24-key pad and an 80-character LCD—or you can use it via its RS-232C port with either an ASCII terminal or a PC. The ICE has 64k bytes of emulation memory, expandable to 512k, and a 4k-frame trace buffer. It lets you examine trace data without halting the μP. The unit also performs 8- and 16-bit emulation of single or multiple EPROM devices to 512k bytes. The logic analyzer, which has a capture memory that's 4k words deep, provides loop and delay counters and four levels of sequential triggering. $3050; μP emulation pods, $300 to $600.

Yu Instruments, 6534 Teakwood St, Cypress, CA 90630. Phone (714) 952-4622. FAX 714-952-4614.

Circle No 351



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- *Includes 16 analog inputs for simultaneous sampling*
- *Provides 32 digital I/O points and 2 DACs*

The CIO-AD16 is an analog/digital input/output card for the IBM PC bus. It incorporates a 16-channel ADC that makes 100k conversions/sec. Even during DMA operation, the card can synchronize external S/H circuits to permit simultaneous capture of data from 16 inputs. The board also contains 24- and 8-bit digital I/O ports and two D/A converters. The card appears to software as two cards, each already widely supported by drivers. Therefore, it is fully compatible with at least seven data-acquisition and -analysis packages as well as with a competitor's high-level-language routines. $799.

Computer Boards Inc, 44 Wood St, Mansfield, MA 02048. Phone (508) 261-1123. FAX 508-261-1094.

Circle No 352

PC PROTOTYPERS

- *Produce single- and double-sided pc boards*
- *Remove conductive material by milling*

The Boardmaker 912 and 912Plus allow you to fabricate prototype single-and double-sided pc boards with a maximum size of 9×12 in. The machines drill holes and mechanically mill away conductive material, eliminating the use of chemicals and photographic processes. They will produce lines as fine as 0.004 in. with spaces as narrow as 0.008 in. The process takes only about an hour for boards of moderate to high complexity. You provide your input in Gerber photoplot format on an IBM PC-compatible 5¼-in. floppy disk. BoardMaker 912, $7000; 912Plus (faster than 912 and providing the highest resolution), $7995.

Instant Board Circuits Corp, 20 Pamaron Way, Suite A, Novato, CA 94949. Phone (415) 883-1717. FAX 415-883-2626.

Circle No 353

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- *Produces 7-nsec-wide pulses to 50 MHz*
- *Lets you control period, width, delay, amplitude, and rise time*

The Model 8500 50-MHz pulse generator produces 7-nsec- to 80-μsec-wide pulses and lets you control pulse period, width, delay, amplitude, and transition time (rise and fall time). The generator, to which the vendor can add a second channel, produces normal, inverted, de-

layed, and double pulses, and provides auxiliary TTL and ECL outputs. You can synchronize the output to an external source and obtain gated pulse bursts. All units contain a counter/timer that measures frequency from 10 Hz to 100 MHz, period from 10 nsec to 50 msec, and pulse width from 50 nsec to 1 sec. \$4995; second channel, \$1995. Delivery, six weeks ARO.

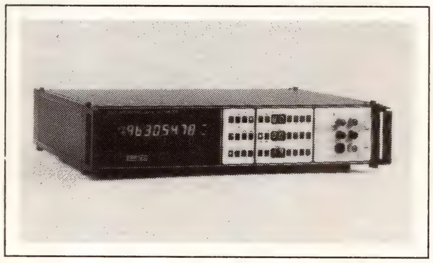
Tabor Electronics Inc, 216 Little Falls Rd, Cedar Grove, NJ 07009. Phone (201) 857-4828. FAX 201-239-7342.

Circle No 354

8½-DIGIT DMM

- *Errors change by 5 ppm/year*
- *Can include 20-channel, 4-wire scanner*

The Model 6048 8½-digit multimeter has a calibration error that drifts no more than 5 ppm/year or 0.5 ppm/day. It measures dc voltage and current, ac voltage and current, and resistance. The unit also performs resistance measurements



at low current. The instrument's input resistance is 10 GΩ. Using integration times from 16.67 msec to 80 sec, its normal-mode rejection exceeds 100 dB at line frequency. Temperature compensation allows the meter to meet its specifications over a 10°C range centered at room temperature. Optionally, the unit can include a 20-channel, 4-wire scanner. \$5300.

Prema Precision Electronics Inc, 4650 Arrow Highway, Suite E-5, Montclair, CA 91763. Phone (714) 621-7292. FAX 714-625-2098.

Circle No 355

PATTERN GENERATOR

- *Produces 4-bit patterns to 2 GHz*
- *Stores 32k-frame sequences*

The PG-2500 pattern generator produces 4-bit-wide pulse patterns to 2 GHz and 8-bit-wide patterns to 1 GHz. The unit can store sequences 4 bits wide by 32k frames deep or 8 bits wide by 16k frames deep. You can shift the outputs (individually in the 1-GHz mode and in pairs in

Text continued on pg 248

National Instruments–Leading a New Generation of Data Acquisition

National Instruments offers a comprehensive line of data acquisition plug-in boards for IBM PC/XT/AT; PS/2 Models 25, 30, 50, 60, 70, and 80; and Macintosh II/IIx/IIcx/SE computers. These boards feature various combinations of analog, digital, and timer inputs and outputs. Standard features include programmable channel sampling order and conversion modes; separate gain for each channel; and pre, post, delayed, analog, and digital triggering–making these boards the most versatile data acquisition products in the industry. Desktop and rack mountable multiplexers can be used to cost-effectively increase the number of analog input channels to 256 per board. A wide variety of signal conditioning modules for thermocouples, RTDs, voltage and current inputs, and high current digital inputs and outputs complete the acquisition hardware line.

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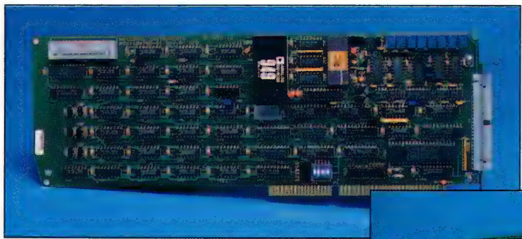
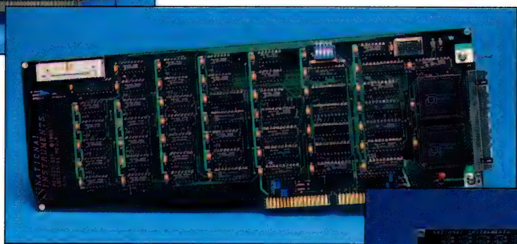
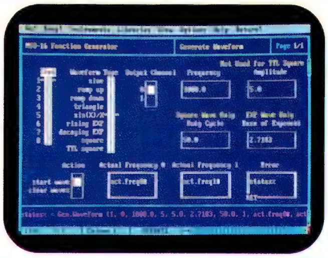


Multifunction I/O Board: AT-MIO-16

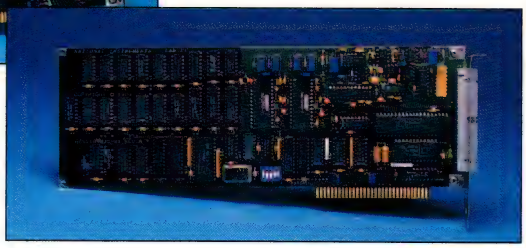
Measure acquires data directly into Lotus 1-2-3 or Symphony spreadsheets.



32-Bit Digital I/O Board: AT-DIO-32F



LabWindows uses function panels to set up data acquisition operations.



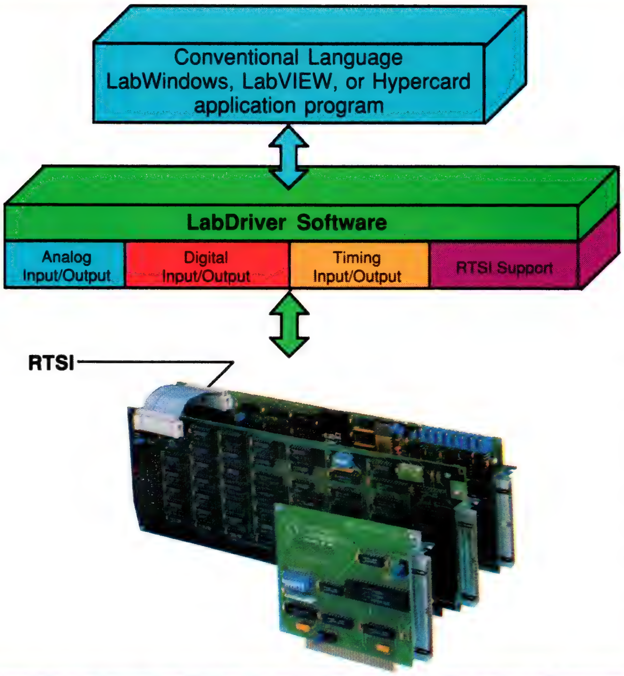
Low cost multifunction I/O Board: Lab-PC

		AT Series Boards					PC/XT/AT
		AT-MIO-16-9	AT-MIO-16-15	AT-MIO-16-25	AT-DIO-24	AT-DIO-32F	Lab-PC (low cost)
Analog Input	Number of Channels	16 SE/8 DI*	16 SE/8 DI*	16 SE/8 DI*			8 SE*
	Resolution	12-bit	12-bit	12-bit			12-bit
	Sampling Throughput (Direct to Memory)	100 ksamples/sec	71 ksamples/sec	45 ksamples/sec			60 ksamples/sec
	Programmable Gain	√	√	√			√
	Pre & Posttriggering	√	√	√			√
	Expandable with Multiplexer	√	√	√			
Analog Output		2	2	2			2
Digital I/O		8	8	8	24	32	24
Counter/Timer		3	3	3			3
RTSI		√	√	√		√	
Software	DOS LabDriver	√	√	√	√	√	√
	LabWindows	√	√	√	√	√	√
	Measure	√	√	√			√

* SE - Single Ended; DI - Differential

Three Generations of Software Technology

National Instruments offers three classes of software to simplify program development tasks. These products represent three generations of programming technology. The first generation is a product called LabDriver that handles the fundamental I/O and data acquisition requirements. The second category includes products that fortify and enhance an existing programming environment by adding high-level data acquisition functions to minimize system development time. The third category, only available on the Macintosh, is a product called LabVIEW. LabVIEW combines the features of the first two with an integrated programming environment and language designed specifically for data acquisition applications.



First Generation

LabDriver™

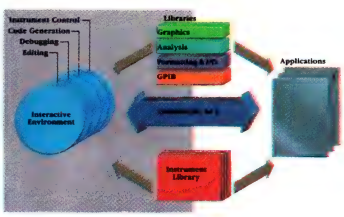
LabDriver is a set of over 50 high-level function calls that program data acquisition plug-in boards for analog input (A/D conversion), analog output (D/A conversion), waveform generation, digital input, digital output, timing input, RTSI, and DMA control from conventional programming languages. National Instruments offers DOS LabDriver for the AT and MC Series boards, NB LabDriver for the NB Series boards, and Lab-SE LabDriver for the Lab-SE.

LabDriver functions are callable from Microsoft QuickBASIC or C on IBM PC/XT/AT and PS/2 computers; and from LightspeedC, MPW C, Lightspeed Pascal, Microsoft BASIC, and HyperCard on the Macintosh.

Examples of LabDriver Functions

AI_Read	AO_Write	DIG_In_Line
DAQ_Start	WF_Start	DIG_Out_Port
SCAN_Start	DIG_Out_Line	DIG_In_Port

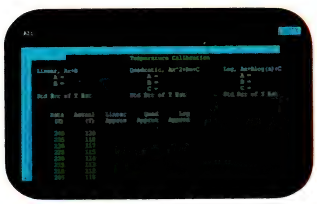
Second Generation



LabWindows®

LabWindows is a set of software tools for developing data acquisition and analysis programs using Microsoft C and QuickBASIC. LabWindows contains extensive libraries for data acquisition, analysis, and presentation, including all functions in LabDriver. Function panels can be used to intuitively control the data acquisition hardware and can also automatically generate Microsoft C or QuickBASIC source code, which can be executed interactively or compiled as a standalone application. The LabWindows libraries are an extensive set of functions for formatting, analyzing, and graphing data. These libraries are used for operations such as digital signal processing and real-time display of acquired data. GPIB and RS-232 capabilities make it easy to integrate standalone instruments into the data acquisition system.

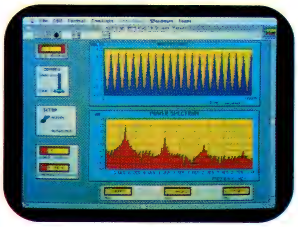
Measure



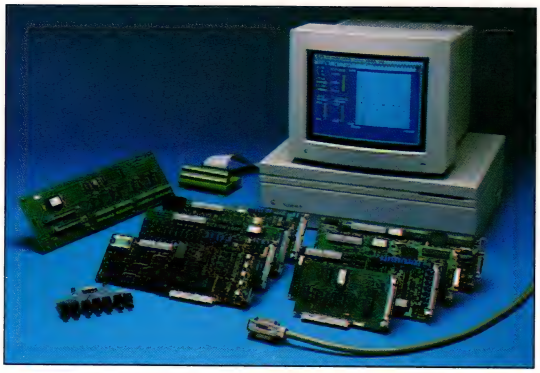
Measure is a set of drivers for Lotus 1-2-3 or Symphony that can control data acquisition hardware and place data directly into a 1-2-3 or Symphony spreadsheet. Measure adds an advanced set of macro commands to perform data acquisition operations easily. Once the data is in the spreadsheet, the full power of 1-2-3 or Symphony can be used to immediately reduce, analyze, and present the data. Measure supports plug-in data acquisition boards for the IBM PC, PS/2, and compatibles, as well as IEEE-488 and RS-232 instrumentation.

The National Instruments selection of data acquisition boards for the Macintosh II, IIx, IIcx, and SE range from a low-cost multifunction board to the highest performing analog input board available on the market. The Macintosh family of boards have sampling rates up to 1 Msamples/sec direct to memory, resolution from 8-bits to 16-bits, and up to six analog output channels.

Macintosh II



LabVIEW is a block diagram programming language for designing virtual instruments that acquire, analyze, and present data.



NB Series Boards

		NB-A2000	NB-MIO-16X	NB-MIO-16	NB-AO-6	NB-DIO-24	NB-DIO-32F	Lab-NB (low cost)
Analog Input	Number of Channels	4 SE(simultaneous)*	16 SE/8 DI*	16 SE/8 DI*				8 SE*
	Resolution	12-bit	16-bit	12-bit				12-bit
	Sampling Throughput (Direct to Memory)	1 Msamples/sec	24 or 55 ksamples/sec	45, 71, or 100 ksamples/sec				60 ksamples/sec
	Programmable Gain		√	√				√
	Pre & Posttriggering	√	√					√
	Expandable with Multiplexer		√	√				
	Analog Output		2	2	6			2
Digital I/O			8	8		24	32	24
Counter/Timer			3	3				3
RTSI		√	√	√	√		√	
DMA		√	√	√	√		√	
Software	NB LabDriver	√	√	√	√	√	√	√
	LabVIEW	√	√	√	√	√	√	√
	HyperLab™		√	√	√	√	√	√
	Paramater Manager Plus		√	√	√	√	√	
	Labtech Notebook			√	√	√	√	

* SE - Single Ended; DI - Differential

National Instruments offers DMA boards to move data directly between hardware and system memory. With a DMA board, both background data acquisition and multichannel, high speed acquisition can occur with the Macintosh II. This allows real-time data acquisition applications to use the host CPU for running the user interface, graphics, and logging to disk while the DMA board and data acquisition hardware acquire data in parallel. With DMA, Macintosh data acquisition systems are able to acquire more channels of data at higher speeds than is possible with the CPU alone.

Block Mode DMA Board: NB-DMA2800

- 32-bit block mode transfers
- Data transfers up to 3.1 Mbytes/sec to Macintosh II memory and 32 Mbytes/sec to block mode memory
- GPIB interface for controlling instrumentation

DMA Board: NB-DMA-8

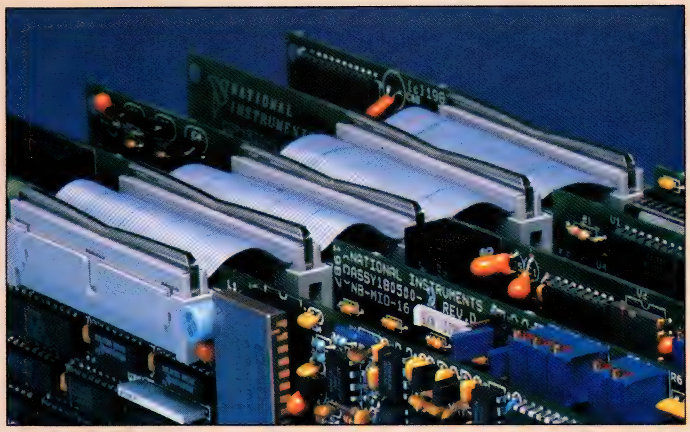
- 32-bit DMA
- Fetch-and-deposit transfers of 8, 16, or 32 bits
- Data rates up to 2.4 Mbytes/sec to Macintosh II memory
- GPIB interface for controlling instrumentation

Macintosh SE

Low-cost Multifunction I/O Board: Lab-SE

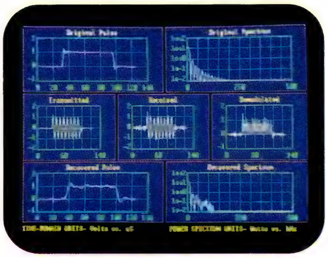
- Integrating 12-bit A/D converter at 15 samples/sec
- 8-bit A/D converter – 8 channels at 125 ksamples/sec
- Two 8-bit D/A converters
- Three 16-bit counter/timers
- 24 digital I/O lines

RTSI™ Bus

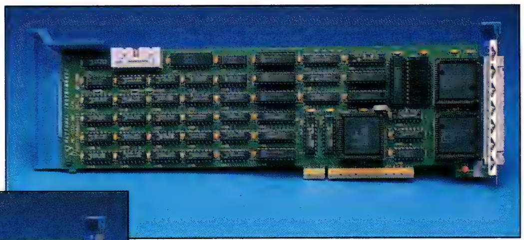


National Instruments expertise in instrumentation led to the development of the Real Time System Integration (RTSI) bus for our data acquisition products. The RTSI bus uses a custom gate array and a ribbon cable to route timing and trigger signals between multiple data acquisition boards. With RTSI, users can synchronize A/D conversions, D/A conversions, digital inputs, digital outputs, and counter/timer operations between multiple boards. For example, with RTSI, two analog input boards can be set up to capture data simultaneously while a third board generates an output pattern, synchronized to the sampling rate of the inputs. RTSI is unique to the National Instruments products and enables plug-in boards and software to be integrated into a complete measurement system.

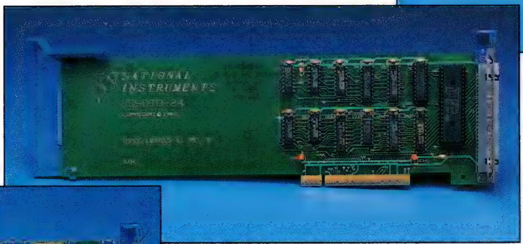
IBM Personal System/2 Micro Channel



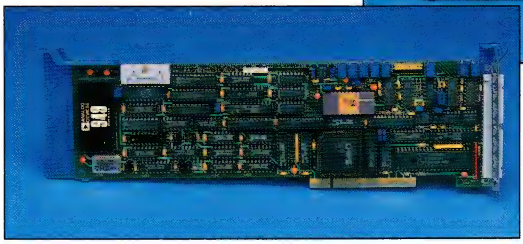
LabWindows analysis and graphics routines process and display acquired signals.



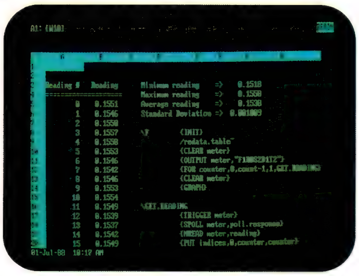
High-Speed 32-Bit Digital I/O Board: MC-DIO-32F



24-Bit Digital I/O Board: MC-DIO-24



Multifunction I/O Board: MC-MIO-16



Measure macros control data acquisition operations from directly within Lotus 1-2-3 or Symphony.

MC Series Boards

		MC-MIO-16-9	MC-MIO-16-15	MC-MIO-16-25	MC-DIO-24	MC-DIO-32F
Analog Input	Number of Channels	16 SE/8 DI*	16 SE/8 DI*	16 SE/8 DI*		
	Resolution	12-bit	12-bit	12-bit		
	Sampling Throughput (Direct to Memory)	100 ksamples/sec	71 ksamples/sec	45 ksamples/sec		
	Programmable Gain	√	√	√		
	Pre & Posttriggering	√	√	√		
	Expandable with Multiplexer	√	√	√		
Analog Output		2	2	2		
Digital I/O		8	8	8	24	32
Counter/Timer		3	3	3		
RTSI		√	√	√		√
Software	DOS LabDriver	√	√	√	√	√
	LabWindows	√	√	√	√	√
	Measure	√	√	√		

* SE - Single Ended; DI - Differential

To design a first class Speakerphone,

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You'll be delighted to find so much sophisticated design already built in.
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Ericsson PBM 3911 and PBM 3912.

- ★ Advanced CMOS design.
- ★ Low power consumption, typically 1mA at 5V.
- ★ Built-in background noise detector.
- ★ Built-in pre-amplifier.
- ★ 0-50dB control range.
- ★ Very accurate ramp control.
- ★ Access to internal control circuits.
- ★ DIP and PLCC packages.

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the 2-GHz mode) over a range of ±2 nsec with 10-psec resolution and an error of <100 psec. You can control the internal clock's frequency in increments of 1% from 10 MHz to 2 GHz. You must use an IBM PC/AT-compatible computer or an 80386-based PC with the industry-standard bus as a host. The computer must have an IBM EGA (enhanced graphics adapter) video controller, a high-resolution color monitor, a hard disk with at least 10M bytes available, and a National Instruments PC 2A IEEE-488 interface. Such a computer can control as many as eight units. $75,000.

Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 350479.

Circle No 356

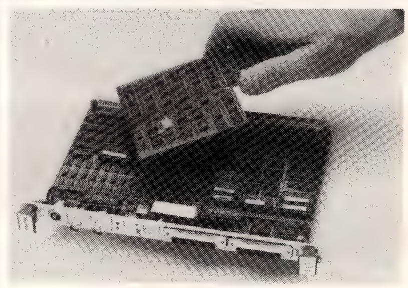
FREQUENCY SOURCE

- *Produces 20V p-p sine waves and TTL square waves*
- *Holds error to 10 ppm from 1 Hz to 100 kHz*

The Wavebox 100 synthesized frequency source produces frequencies from 1 Hz to 100 kHz with 1-Hz resolution and 10-ppm error. You dial in the output frequency on thumbwheel switches. The unit produces two outputs: a TTL/CMOS-level square wave and a variable-amplitude sine wave (20V p-p max) whose offset you can adjust over a ±10V range. The total harmonic distortion of the sine wave is at least 40 dB below the output level. $325.

Teledata Systems, 68 Reservoir Rd, New Milford, CT 06776. Phone (203) 355-8285.

Circle No 357



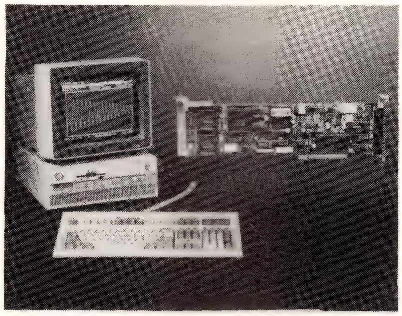
VMEBUS TRACER

- *Adds complex triggering to state and performance analysis*
- *Reports protocol violations via ASCII terminal*

The VBAT-321-Piggyback is a board you add to the vendor's VBT-321 advanced VMEbus tracer. The piggyback board enables the bus tracer to trigger on a large number of bus timing and protocol violations. Unlike the vendor's VBAT stand-alone VMEbus anomaly trigger unit, which reports error conditions on a series of LEDs, the VBT-321/VBAT-321-Piggyback combination displays the problems it finds on an ASCII terminal. Like the VBAT, the piggyback unit continuously monitors 98 bus lines and simultaneously checks for 104 types of errors. Piggyback, $2500; bus tracer, $5990.

VMEtro Inc, 2500 Wilcrest, Suite 550, Houston, TX 77042. Phone (713) 266-6430. FAX 713-266-6919.

Circle No 358



PS/2 I/O CARDS

- *Feature Micro Channel compatibility*
- *Perform A/D and D/A conversion*

The PCI-601W and PCI-602W are data-acquisition boards for the Micro Channel Architecture bus of the IBM PS/2 models 50, 60, 70, and 80. Both boards incorporate 16 single-ended or eight differential analog inputs; a 12-bit ADC, which takes 70k samples/sec; a programmable-gain amplifier with gains of 1, 10, 100, and 1000; programmable channel scanning; two independent 16-bit counters that you can cascade or use to measure period and frequency; and 16 digital I/O lines. In addition, the PCI-602W has a pair of 16-bit D/A outputs that you can update as fast as 250,000 times each second. The input scanner allows burst-mode operation, in which the ADC scans selected channels in rapid succession and then waits before acquiring additional samples. PCI-601W, $995; PCI-602W, $1195; software drivers, $180 each.

Burr-Brown Corp, 1141 W Grant Rd, MS 131, Tucson, AZ 85705. Phone (602) 746-1111. FAX 602-623-8965.

Circle No 359

ACQUISITION SYSTEM

- *Makes 1000 15-bit measurements/sec*
- *Stores 75,000 readings*

The 2287A Helios Plus is an analog front end for PC-based data-acquisition systems. You can choose among the ADCs the system contains: a 15-bit unit takes 1000 sam-

ples/sec; a 17-bit unit takes 16 samples/sec. The system accommodates as many as 1000 channels. It communicates with the host computer at 19.2k bps max via an RS-232C port. A buffer can store as many as 75,000 readings, enabling the system to acquire a large number of samples and transmit them after acquisition. Several PC-based software packages, including Labtech Notebook, LT/Control, and Measure, support the hardware. From \$3500. Delivery begins January 2, 1990.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853.

Circle No xxx

Philips Test and Measurement, Bldg HKF, 5600 MD, Eindoven, The Netherlands. Phone local office.

Circle No 360

I/O MODULES

- *Measure 1.8×3.9 in.*
- *Plug onto VMEBus and Nubus boards*

The Industrypack modules are 1.8×3.9-in. pc cards that plug onto VMEbus and Nubus boards to perform data-acquisition functions. The IP-Precision ADC is a miniaturized subsystem with 20 single-ended or eight differential channels. It directly accepts low-level inputs from thermocouples, strain gauges, and resistive bridges and makes 65,000 12-bit conversions/sec. The unit also contains a precision reference and a D/A converter. The IP16-DAC incorporates three 16-bit D/A converters. The IP-DAC contains six 12-bit D/A converters. The IP-488 is a miniaturized IEEE-488 controller. IP-Precision ADC, \$523; IP16-DAC, \$540; IP-DAC, \$428; IP-488, \$244.

GreenSpring Computers Inc, 1204 O'Brien Dr, Menlo Park, CA 94025. Phone (415) 327-1200. FAX 415-327-3808.

Circle No 361

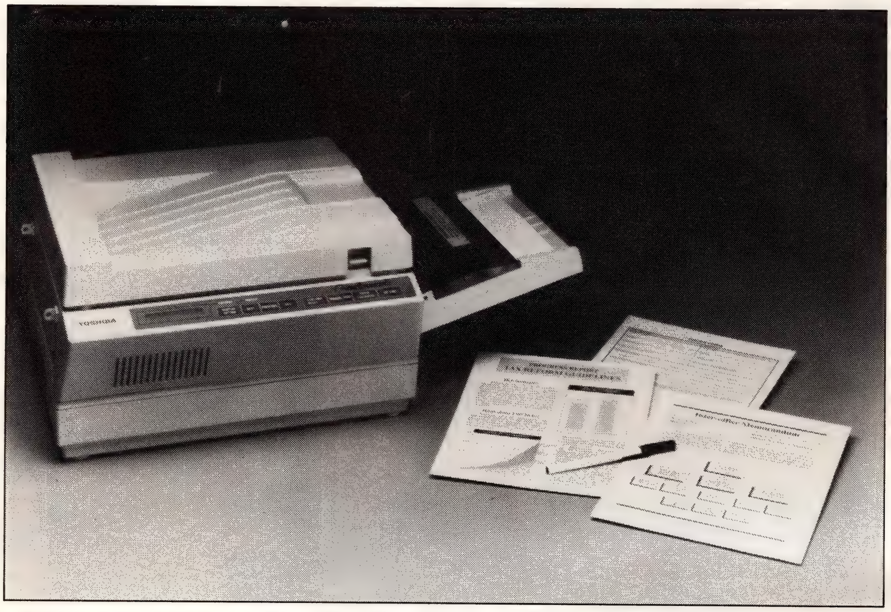

RUSH
SILKSC
USH JOB
COMPONENT SIDE ETCH
74HCT08
74HCT04
NONINVERTED 3 STATE BUFFER
QUAD 2-INPUT POS-AND GATES
HEX INVERTERS
8251A
10K RES NET
10 PIN RESISTOR PACKAGE
74HC00
HD3-4702-9
QUAD 2-INPUT NAND GATE
74HC164
0.1UF
8-BIT PAR. OUTPUT SER SHFT REG
BYPASS CAPACITORS
Bob,
Who can route this board faster and more economically?
Calay?
Mentor? Very Pricey!
Daisy? $$
CADSTAR?

NEW PRODUCTS

COMPUTERS & PERIPHERALS

LASER PRINTER

- *Compatible with HP's Laser Series II printers*
- *Has a graphics resolution of 300×300 dpi*



The PageLaser6 laser printer is compatible with HP's LaserJet Series II printers, font cartridges, and soft fonts. The printer also emulates an IBM Proprinter XL24 printer. You can communicate with the unit through a Centronics parallel port or an RS-232C port. Resident fonts include Courier, Courier Bold, Prestige Elite, and Line Printer. The device has a suggested usage rate of 4000 pages/month and prints letter-size pages at 6 pages/minute. Its standard memory configuration is 512k bytes with options for 1M, 2M, and 4M bytes via expansion board. Printing graphics at 300×300-dpi resolution, the unit has a printer life of 300,000 pages. Its input and output trays can each hold 150 sheets. The printer measures 16.1×15.4×8.3 in. and weighs 35 lbs. $1899.

Toshiba America Information Systems Inc, Computer Systems Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (800) 457-7777; in CA, (714) 583-3000.

Circle No 362

IBM VGA BOARD

- *Computer and VGA 15-pin monitors for IBM PCs*
- *Provides 16 colors from a palette of 262,144*

You can use the IBM VGA adapter board for the IBM PC, PC/XT, PC/AT, and compatible computers with VGA 15-pin color or monochrome monitors. It's backward compatible with IBM EGA, IBM CGA, and IBM MDA, as well as Hercules graphics standards. An autoswitch feature automatically adjusts the card to the graphics mode. The board comes with 256k bytes of RAM and delivers 640×480-pixel resolution with 16 simultaneous colors from a palette of 262,144. An optional resolution of 320×200 pixels provides 256 simultaneous colors. The text resolution is 80 columns×25 lines. You can use the board in either an 8- or a 16-bit expansion slot. The board utilizes a Chips and Technologies graphics chip and requires no jumpers or switches to be set during installation. $345.

Boca Research Inc, 6401 Congress Ave, Boca Raton, FL 33487. Phone (407) 997-6227. FAX 407-997-0918. TLX 990135.

Circle No 363

I/O CARD

- *Provides four RS-232C communications ports*
- *Uses Z85C30 chip for synchronous and asynchronous protocols*

Providing four RS-232C communications ports, the LPM-7314 CMOS STD Bus card uses the Z85C30 serial-communications-controller IC for multiprotocol asynchronous and synchronous communications. Each channel operates independently and is capable of 38.4k asynchronous baud rates and 307.2k synchronous baud rates. Each channel provides modem-handshake control lines. Programmable loop-back mode and auto echo are available on each channel. The card works with Z80 and 80X88 µPs, and a driver utility is available for DOS-based STD Bus systems. The all-CMOS board consumes 420 mW and operates from −40 to +85°C. $395; NMOS version for the TTL STD Bus, $300.

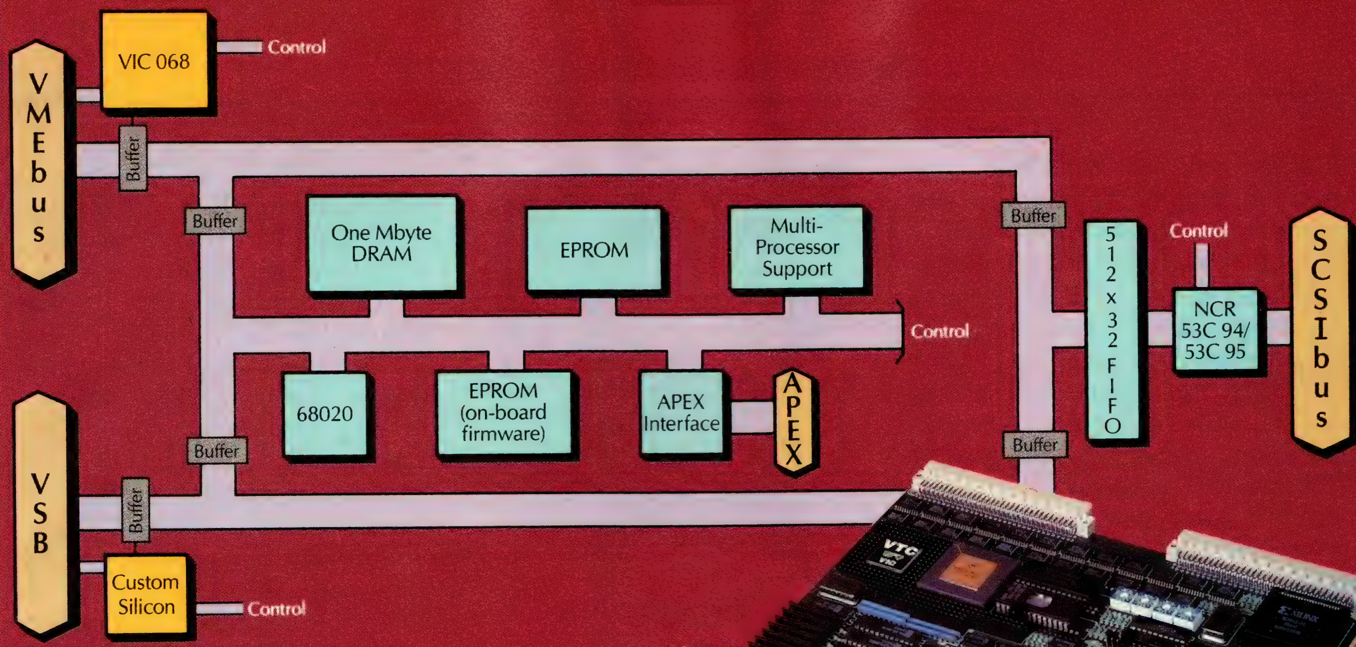
WinSystems Inc, Box 121361, Arlington, TX 76012. Phone (817) 274-7553. FAX 817-548-1358.

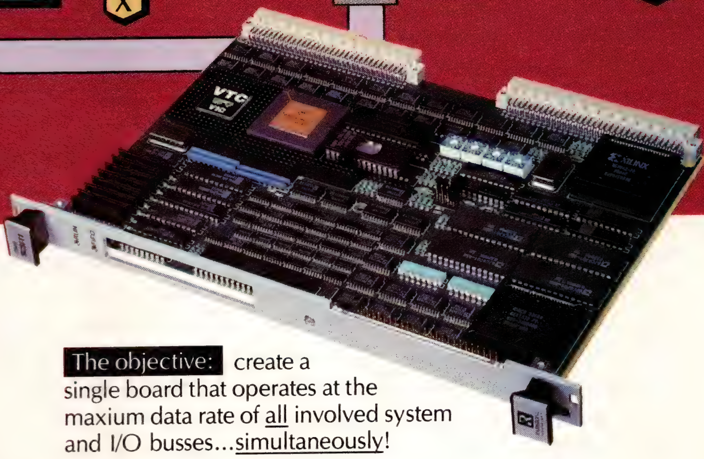
Circle No 364

ETHERNET BOARD

- *Interfaces to two independent LANs*
- *3-bus architecture and 5-port memory eliminate wait states*

The TSVME-551 Ethernet adapter board for the VMEbus uses a 16-MHz 68020 µP to interface with two independent Ethernet LANs. A triple-bus architecture, a 1M-byte 5-port memory, and a burst-mode





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- A full master/slave VSB interface with its own sustained 30 Mbytes/sec. DMA transfer rate
- 68020 Microprocessor
- 1 Mbyte Quad-ported DRAM
- APEX (Advanced Processor EXtension bus) to add the functionality you want–Ethernet, second SCSI, IEEE 488, floppy, parallel I/O...or your own.

Commercial through Mil-Spec

Radstone offers an entire family of SCSI interface boards for applications from commercial through full Mil-Spec. Plus the industry's best selection of commercial, ruggedized and military VME processor, memory, communications, I/O and controller boards, development systems and software. Radstone has your VME system solution now. Call us for the details.

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Germany Bahnhofstraβe 38, D-6090 Rüsselsheim (0 61 42) 6 80 04

RADSTONE
TECHNOLOGY

CIRCLE NO 191

VMEbus controller eliminates wait states during data transfer. Its μP executes instructions from either 256k or 512k bytes of local RAM concurrently with DMA burst transfers to the VMEbus and Ethernet transfers to the shared memory. The μP, both Ethernet controllers, and the VMEbus can access the shared memory. Its DMA controller uses a command FIFO device to stack as many as 32 transfer commands. A separate 2k-byte data buffer allows the DMA operation to be independent of other onboard resources. The board transfers data at 10M bps on both Ethernet controllers even when all the memory ports are active. Single-port version, $2996; dual-port version, $3746 (100).

Themis Computer, 6644 Owens Dr, Pleasanton, CA 94566. Phone (415) 734-0870. FAX 415-734-0873.

Circle No 365

LAPTOP COMPUTER

- *Uses an 80386SX μP running at 16 and 8 MHz*
- *Has 2M bytes of RAM and supports external monitors*

The LapPRO-386SX laptop computer uses an 80386SX μP running at 16 or 8 MHz and provides 2M bytes of RAM that's expandable to 4M bytes. Its 75-key keyboard provides 12 function keys when you activate the FUNC key. The monitor port supports IBM CGA, IBM EGA, and IBM VGA external monitors. Standard features include a 40M-byte hard-disk drive with 28-msec access time, a 3½-in. floppy-disk drive, two serial ports, a parallel port, a blue-on-white LCD, and a numeric keyboard. Options include a 2400- or 4800-baud internal modem, a coprocessor, a 100M-byte hard-disk drive, external floppy-disk drives, and an external keyboard port. The device can operate from a 110 or 220V power supply, a 12V car lighter, or a battery pack. The unit measures 15.94×12.6×3 in. and weighs 13 lbs without a battery and 16.5 lbs with a battery. $4995.

Dauphin Technology Inc, 1125 E St Charles Rd, Lombard, IL 60148. Phone (312) 627-4004. TLX 297246. FAX 312-627-7618.

Circle No 366

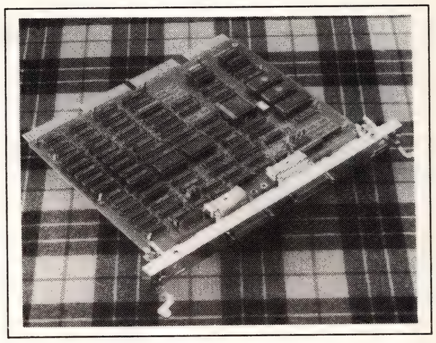
CPU BOARD

- *Uses Intel 960CA RISC μP for VMEbus*
- *Provides Ethernet, SCSI, parallel port, and four RS-232C ports*

The HK80/V960E VMEbus CPU board uses Intel's 960CA RISC μP. The μP includes a 1k-byte instruction cache, a 1k-byte static data RAM, and a 4-channel DMA controller. Delivering six native MIPS and 30 VAX MIPS, the board also uses a 2-way interleaved architecture, which provides zero-wait-state access to either 2M or 8M bytes of onboard 70-nsec dual-port SRAM. In addition, the board has 1M byte of EPROM and 128 bytes of nonvolatile RAM for storing user-defined configuration data. The board has an Ethernet interface, a SCSI, a parallel port, and four RS-232C ports. The device uses the VIC068 VMEbus interface IC, which provides transfer speeds as fast as 40M bytes/sec. Running the VxWorks operating system, the board lets designers develop application code on a Unix host such as a Sun workstation. The board is currently in beta site with production units scheduled for the first quarter of 1990. 33-MHz version with 2M bytes of RAM, $2795 (100).

Heurikon Corp, 3201 Latham Dr, Madison, WI 53713. Phone (800) 356-9602. FAX 608-831-4249. TLX 469532.

Circle No 367



PRINT ACCELERATOR

- *Provides DMA printer interface*
- *Operates with VMS and RSX11M software drivers*

The Sprint It printer accelerator for the MicroVAX provides a buffered DMA printer interface for the Q Bus. Its features are transparent to the operating system so it runs with VMS and RSX11M software drivers. The unit connects to printers with Centronics, Dataproducts, or RS-232C interfaces. The board accepts data into its 64k-byte data buffer at a 500-kHz rate, and the printer controls the throughput from the board to the printer. The quad-size board's I/O page address is programmable from 760000 octal to 777770 octal. The board presents one standard dc and two standard ac loads to the Q Bus and draws 2A from the 5V supply. Versions

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for single and three phase applications where high efficiency, precise regulation and a high degree of packaging density are required.

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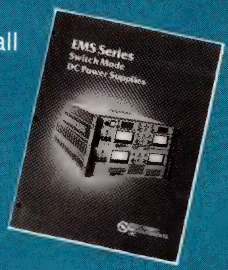
Want all the details on the small and the mighty? Write or call for the latest Tech Bulletin on the EMS Series of DC Power Supplies.



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*Except in New Jersey, Alaska, Hawaii and Canada call (201) 922-9300.

See us at WESCON Booth #639 & #641

CIRCLE NO 193

are available for the MicroPDP 11 series and the MicroVAX I, II, and III computers. Low-speed version for line printers with speeds of <1000 lpm and page printers with speeds of <15 pages/minute, $1500; high-speed version, $2000.

Tartan Technical Inc, 321 Billerica Rd, Chelmsford, MA 01824. Phone (508) 250-9341. FAX 508-250-0567.

Circle No 368

LCD TERMINAL

- *Replaces CRT terminal in space-limited applications*
- *Has active screen area of 4 × 9 in.*

The CDS700-P LCD Terminal is designed to replace a CRT terminal in space- and power-limited applications. The unit measures 6.5 × 11 × 1.5 in., has an active screen area of 4 × 9 in., and draws 250 mA from a 5V supply. Optional white fluorescent or EL backlighting consumes an additional 1 to 5W, depending on intensity. You interface to its onboard LCD controller through an RS-232C port. Additional features include 25 lines of 80 characters; double-high and double-wide characters; block graphics and graphics primitives; full cursor control; video memory; paging and scrolling; an IBM PC/XT or a parallel ASCII keyboard interface; and a bell tone. $995.

Communications and Display Systems Inc, 182 Morris Ave, Holtsville, NY 11742. Phone (516) 654-1143.

Circle No 369

FAX CARD

- *Has two facsimile transceivers*
- *Host transmits/receives data over as many as 12 channels*

The TR112 FAX board for the IBM PC/AT and compatible computers contains two facsimile transceivers for multichannel fax applications. The board doubles the number of channels that the host system can accommodate. The board's autorouting scheme takes advantage of the direct inward dialing (DID) provided by telephone companies that allows outside callers to dial internal extensions directly. An optional digital-voice-response capability lets the board retrieve and play back digital speech previously recorded on a disk drive. This capability along with DTMF tone detection can implement integrated voice response in fax applications. Other features include Group 3 compatibility, ASCII text to fax-format conversion, and multiple-type fonts. Without autorouting, $1995; with autorouting, $2495.

Brooktrout Technology Inc, 110 Cedar St, Wellesley Hills, MA 02181. Phone (617) 235-3026. FAX 617-235-0310.

Circle No 370

COMMUNICATIONS CARD

- *Transfers data to 16 asynchronous devices*
- *Designed for Unix and X-windows graphics systems*

The 781 serial-communications-controller card for the VMEbus allows a VMEbus host to communicate with as many as 16 asynchronous devices. The board is designed to take advantage of the features in Unix and X-windows graphics systems. Each device can operate independently at data-transfer rates of 100 to 38.4k baud. Because the board has a character throughput of 320k bps, it can communicate at 19.2k baud to 16 devices simultaneously. The 6U form-factor board contains a 10-MHz 80186 μP and a 64k-byte buffer. Two octal receiver/transmitters handle the asynchronous communications protocols. The μP handles the tasks of DMA setup and execution, flow control, and interrupt servicing. $1795.

Xylogics Inc, 53 Third Ave, Burlington, MA 01803. Phone (617) 272-8140.

Circle No 371

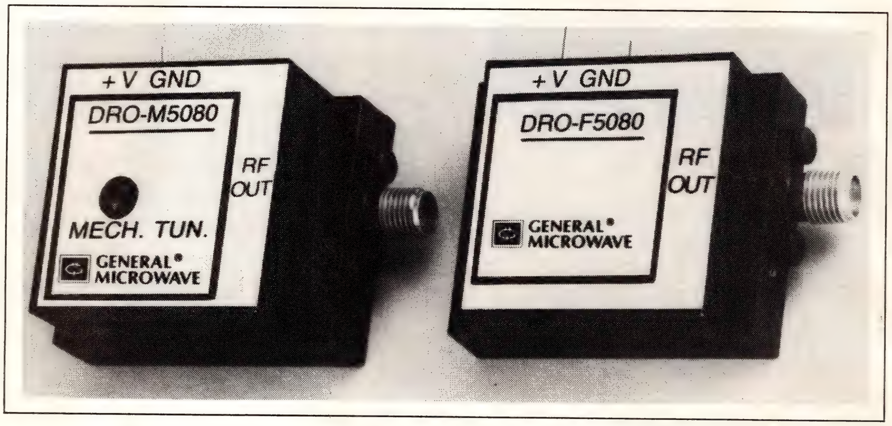
NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

OSCILLATORS

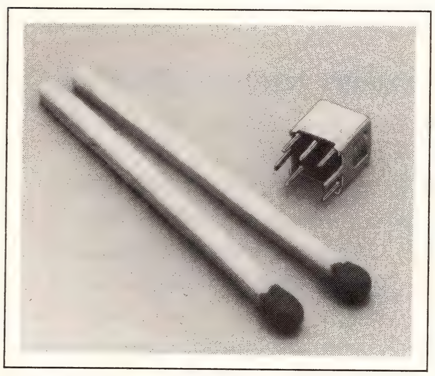
- *Stability equals 1 ppm/°C max*
- *Have a 10-dBm output*

Series 5000 fixed-tuned and mechanically tuned dielectric resonant oscillators cover a 5- to 18-GHz frequency range. The frequency stability of the fixed-tuned model at 18 GHz equals 1 ppm/°C max, and maximum frequency pulling and pushing measure 150 and 7 kHz, respectively. RF power output is at least 10 dBm and varies only ±1 dB over the −54 to +85°C operating range. Phase noise is at least −85 dBc at a 10-kHz offset. Second harmonic and nonharmonic spurious responses are at least −30 and −70 dBc, respectively. All oscillators are supplied with removable surface-mount-assembly female output connectors. Fixed-tuned version, $1500; mechanically-tuned version, $1600.



General Microwave Corp, 5500 New Horizons Blvd, Amityville, NY 11701. Phone (516) 226-8900.

Circle No 372



VARIABLE INDUCTOR

- *Available in two ranges*
- *Designed to accommodate wave-soldering operations*

The 5P miniature shielded variable inductor is designed for IF-circuit and oscillator applications. The device is available in two frequency/inductance ranges: 200 kHz to 2 MHz (30 μH to 1 mH) or 1 to 15 MHz (1 μH to 40 μH). Measuring just 6 mm high and 6 mm square, the inductor has a patented design that features a cup core adjuster threaded directly into the shield, permitting the use of a larger cup core and drum core. Other features include corner standoffs to prevent device tilting during wave soldering, a waxed core to prevent core-lock during fluxing and soldering operations, and a plated brass housing for better magnetic shielding. $0.86 (1000). Delivery, 12 weeks ARO.

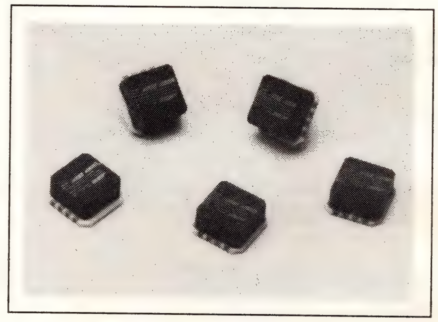
Toko America Inc, 1250 Feehanville Dr, Mount Prospect, IL 60056. Phone (312) 297-0070. FAX 312-699-7864.

Circle No 373

PRESSURE SENSOR

- *Designed for surface-mount applications*
- *Measures absolute pressure*

The Model 1431 solid-state, piezoresistive pressure sensor is housed in a miniature surface-mount package. The design is based on a silicon chip that consists of a micromachined silicon diaphragm with a piezoresistive 4-arm active Wheatstone bridge. Measuring only 0.3×0.3 in. and weighing 0.3g, the sensors are available in absolute pressure ranges of 15 to 300 psi full scale. The device operates from either a constant current or constant voltage supply and is accurate to >±0.25%. The typical full-scale output span equals 60 mV. Alternate packages are available for applications requiring gauge or differential pressure measurements. From $16.



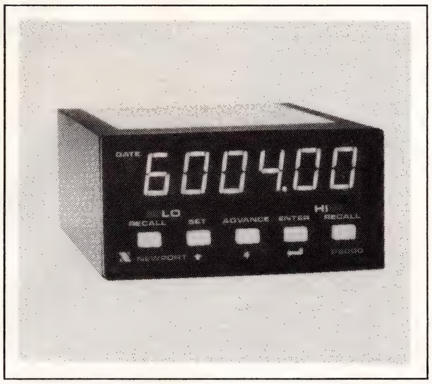
IC Sensors Inc, 1701 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1800.

Circle No 374

PROCESS METER

- *Offers programmability*
- *Includes integral RAM*

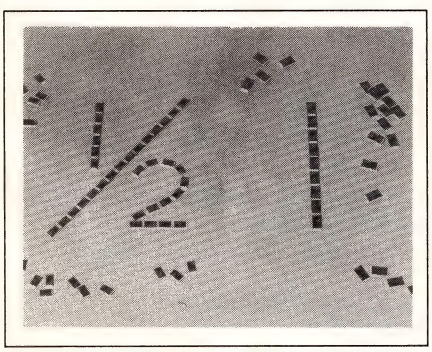
You can program the P6004 microcomputer-based, 6-digit, ⅛DIN panel instrument as a flow-rate indicator/controller or an accumulating flow indicator/controller. The 6004 incorporates a V/F converter that accepts the 4- to 20-mA, 0 to 10V, or 0 to 2V analog input. The P6000 version accepts pulse signal



inputs. Programmable features include a 6-digit scale factor, a 6-digit offset or preset device, and two on/off setpoints with open-collector outputs for control or alarm. All setup information is stored in nonvolatile RAM. Four levels of program lockout provide for program security. An RS-232C interface with modem support is standard. P6004, $374; P6000, $275.

Newport Electronics Inc, 2229 S Yale St, Santa Ana, CA 92705. Phone (714) 540-4914. FAX 715-546-3022. TWX 910-595-1787.

Circle No 375



CHIP RESISTORS

- *Handle as much as 1W of power*
- *Tolerance is as low as 1%*

Models CRCW 2010 and 2512 thick-film chip resistors handle power levels of ½ and 1W, respectively, and are available with tolerances of ±5 and ±1%. CRCW 2010 units are available with resistance values of 3Ω to 320 kΩ, and you can order them with temperature coefficients

of ±300 or ±200 ppm/°C. The resistance range for CRCW 2512 devices spans 3Ω to 240 kΩ; temperature coefficients equal ±300, ±200, or ±100 ppm/°C. The resistors feature wraparound terminations. A special nickel barrier serves to protect the inner electrodes and ensure reliable soldering. Designed for use with automatic placement equipment, the units are available in 12-mm tape-and-reel or bulk packaging. For 4000-piece reel of CRCW 2010 unit (5% tolerance with a resistance of 10Ω to 240 kΩ), $0.32; for a 2000-piece reel of CRCW 2512 unit (5% tolerance, with a resistance of 10Ω to 240 kΩ resistors), $0.33. Delivery, eight weeks ARO.

Dale Electronics Inc, 2064 12th Ave, Columbus, NB 68601. Phone (402) 371-0080.

Circle No 376

DIP SWITCHES

- *Offer as many as 10 positions*
- *Surface-mount style available*

The A3000 DIP is an spst DIP-type switch that provides a choice of as many as 10 switching positions. Three versions are available: the A3001 with 15° inclined leads, the A3003 with parallel leads, and the A3002 surface-mount version that features gull leads. Plug-in versions are compatible with automatic insertion equipment, and all three versions are immersion washproof and will accommodate ultrasonic cleaning procedures. The switch has a positive slide action, which produces good contact wiping action. Two of the package corners are beveled to facilitate the removal of the sealing tape. Standard versions come with 4, 5, 8, or 10 on/off switches. Other versions are available on request. $1 (1000) for an 8-position unit. Delivery, stock to eight weeks ARO.

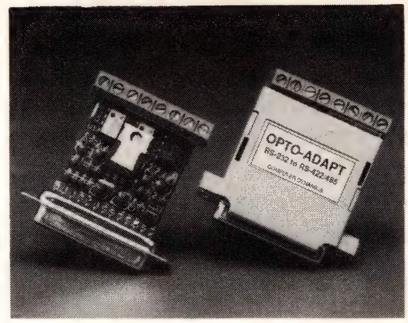
Siemens Components Inc, 186 Wood Ave S, Iselin, NJ 08830. Phone (800) 222-2203.

Circle No 377

ADAPTER

- *Provides optical isolation*
- *Needs no external power*

The Opto-Adapt optically isolated adapter plugs into any RS-232C DB25 male connector and converts the transmit and receive signals to RS-422 levels. The RS-422 cable connects to the adapter through a terminal strip. Power for the converter's RS-232C side is derived from the RS-232C signal lines. Power for the RS-422 side is supplied by an external 8 to 15V supply, which connects to the terminal strip. Data-communications-equipment and data-terminal-equipment configurations are jumper selectable. The adapter comes equipped with a female 25-pin RS-232C connector. A transmitter disable function is available as an option. $120; external power supply, $10.



Computer Dynamics Sales, 107 S Main St, Greer, SC 29650. Phone (803) 877-8700. FAX 803-879-2030.

Circle No 378

DC/DC CONVERTERS

- *Rated for 200W*
- *Available in a shielded case*

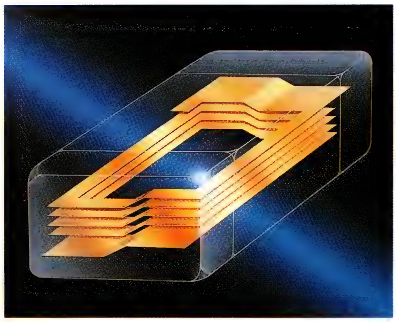
EMQ Series dc/dc converters offer power output ranging from 75 to 200W. They accept 10 to 300V inputs and provide outputs of 5 to 48V. The units automatically latch off for any overvoltage or baseplate overtemperature condition. An aluminum baseplate allows the converters to provide 50W outputs without airflow or heat sinks when mounted on pc boards. The converters can be paralleled for increased power output or operated in the N+1 mode for system redundancy. They also have provisions for remote sense, voltage adjust, and external synchronization. You can order the converters in an insulated and metalized case, which creates a 6-sided RFI shield. $95 to $175 (100).

Electronic Measurements, 405 Essex Rd, Neptune, NJ 07753. Phone (201) 922-9300.

Circle No 379

TDK TOTAL SURFACE MOUNT TECHNOLOGY

In Surface Mount Technology, It's What's Beneath The Surface That Counts



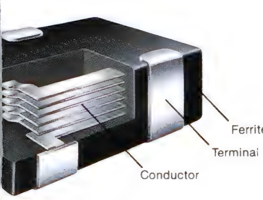
TDK puts you at the leading edge of today's most important surface mount technology developments—from a full range of multilayer SMDs to complete automatic mounting systems. Waiting inside is your introduction to TDK's Total Surface Mount Technology.

TDK®

nd Mounting Systems Apply Lea

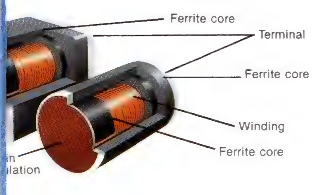
ip Transformer

ip transformer has absolutely no
TDK advancements in magnetic
ive materials, and multilayer
ansformer features a completely
with inherent magnetic shielding.



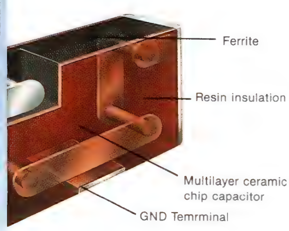
ductor (Wound Micro Chip Inductor)

was developed to combine
high inductance up to 1000μH.
ed magnetic circuit structure
ic shielding, making this chip
mounting applications. It features
and achieves a high Q factor.



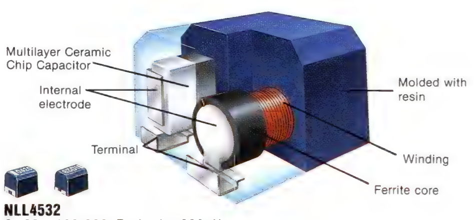
MI Filter

MI Filter, ACF Series, is a
e chip bead and multilayer ceramic
h has an attenuation of over
650MHz frequency range and
construction accounts for its
shielding characteristics.
e the Micro Chip EMI Filter,
1.8mm (.07 inch) thick, it
h for



Leadless EMI Filter (Wound Chip EMI Filter)

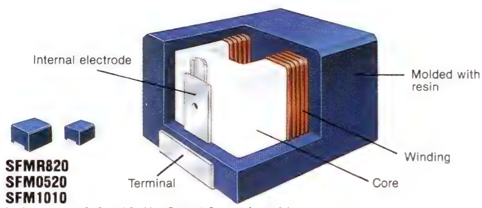
The rendering of the EMI filter into a chip format has been considered essential for the creation of the smallest and lightest electronic products. TDK was one of the first to do it. Our leadless EMI filter is effective against EMI in signal lines, and has been designed for good solderability, thermal resistance, moisture resistance, and mechanical strength.



NLL4532
C: 33 ~ 100,000pF L: 1 ~ 220μH

Leadless Line Choke SF Coil
(Wound Chip Line Choke)

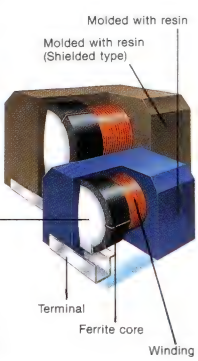
By employing advanced winding technology, TDK has developed magnetic material with excellent absorption of thyristor switching noise. Molded in resin, they are ideal for eliminating EMI in power supply lines for digital circuits.

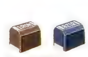


SFMR820
SFM0520
SFM1010
Inductance: 0.8 ~ 10μH Rated Current: 1-2A

Leadless Inductor/Power-Line Leadless Inductor (Wound Chip Inductor)

TDK's advanced winding technology together with compact ferrite cores with highly precise performance characteristics are what make TDK Leadless Inductor unique. Power-Line Leadless Inductor is ideal for EMI suppression in power lines with 60 ~ 1800mA current rating. Both feature metal terminals and come molded in resin for maximum reliability.

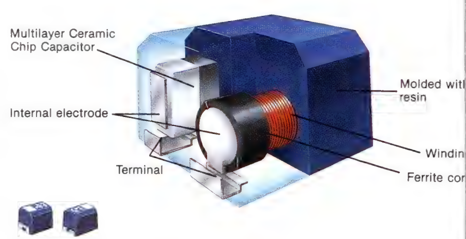




NL322522 L: 0.01 (450) ~ 220μH (50mA)
NL453232 L: 1.0 (450) ~ 1,000μH (30mA)
NL565050 L: 1,200 (75) ~ 10,000μH (25mA)
NLF453232 L: 1.0 (150) ~ 1,000μH (15mA)
[Shielded Inductor]
NLC322522 L: 1.0 (850) ~ 330μH (60mA)
NLC453232 L: 1.0 (1050) ~ 220μH (120mA)
NLC565050 L: 1.0 (1,800) ~ 1,000μH (85mA)

Leadless LC Trap (Wound Chip LC Trap)

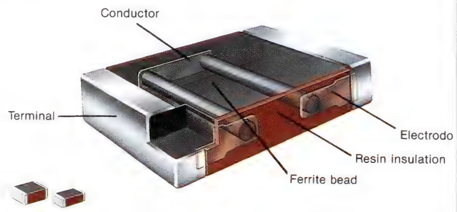
TDK's LC trap is a composite consisting of a miniature coil and a multilayer ceramic chip capaci
A new proprietary structural design affords high
accurate dimensional control, making this chip w
suited for fully automated mounting systems.
Metal terminals insure excellent solderability.



NLT4532
F range: 630kHz ~ 13MHz
Tolerance: ±2% Attenuation: 20dB min.

Ferrite Chip EMI Suppressor

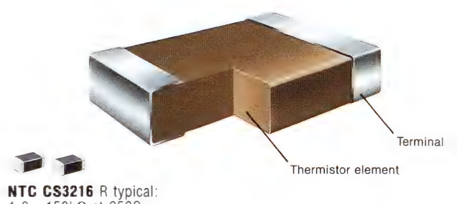
This chip EMI suppressor features proprietary m
materials and incorporates the latest advances i
chip technology. The device effectively eliminat
EMI and prevents parasitic oscillation. A TDK
proprietary structural design insures high impeda
per volume, and coverage over a wide frequenc
range.



CB201209 Zo: 7, 10, 11Ω
CB321611 Zo: 19, 26, 31Ω
CB322513 Zo: 31, 52, 60Ω
CB453215 Zo: 70, 120, 125Ω

NTC Chip Thermistor

The Negative Temperature Coefficient chip thermistor is a temperature compensation devic
Although in chip form, it has the same basic
performance characteristics as conventional lead-ty
NTC thermistors. The NTC chip thermistor can
also be utilized to make a temperature compensat
circuit on a PC board. Nominal resistance and
temperature characteristic tolerances have been
reduced to extremely low levels.



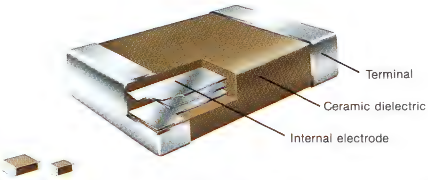
NTC CS3216 R typical:
1.0 ~ 150kΩ at 25°C
Temp. Range: −25 ~ +85°C

TDK SMDs a

Simplifying High Density Placement-TDK Surface Mount Devices

Multilayer Ceramic Chip Capacitor

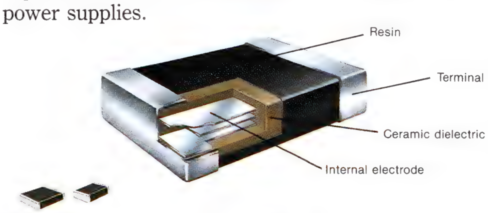
This line of capacitors offers a wide range of capacitances, temperature characteristics, and sizes, with terminals designed for excellent solderability. As a leading manufacturer of ceramic capacitors, TDK remains committed to bringing you the highest possible product reliability and stability at all times.



C1608 (CC0603) C: 0.5 ~ 22,000pF **C3225** (CC1210) C: 750 ~ 470,000pF
C2012 (CC0805) C: 0.5 ~ 100,000pF **C4532** (CC1812) C: 2,400pF ~ 1μF
C3216 (CC1206) C: 0.5 ~ 220,000pF **C5650** (CC2220) C: 5,100pF ~ 1.5μF

Large-Capacitance Multilayer Ceramic Chip Capacitor

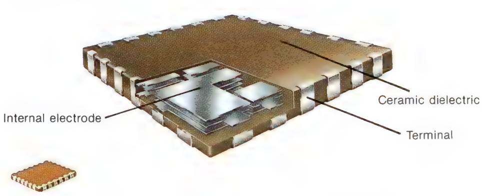
Large-capacitance multilayer ceramic chip capacitor covers the capacitance range normally associated with electrolytics. It features a non-polarized construction and a long life. This large-value capacitor is seeing widespread use in switch-mode power supplies.



HC8050 C: 1 ~ 6.8μF **HC1280** C: 2.2 ~ 22μF
HC1063 C: 1.5 ~ 10μF **HC1612** C: 4.7 ~ 47μF
TC: +20, −30% (−25 ~ 0 + 25 ~ +85°C)

Multilayer Ceramic Chip Capacitor Network

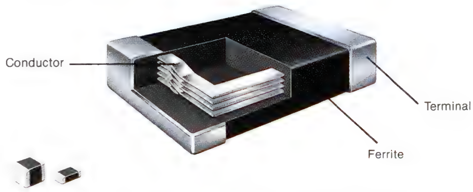
Through advanced multilayer and integration processes, TDK can incorporate a network of 12 ceramic capacitors into a single chip, with your choice of capacitances and interconnection topologies. In addition, these networks are made of high-performance insulating materials, allowing other chips to be mounted directly onto the surface. This provides compatibility with the new generation of hybrid chip designs.



MCN7575
TC; COH, 1 ~ 100pF (12 capacitors) Class II, 100 ~ 470,000pF
; SL, 10 ~ 1,000pF (TC: −1,000, +350ppm/°C) (12 capacitors)

Multilayer Chip Inductor

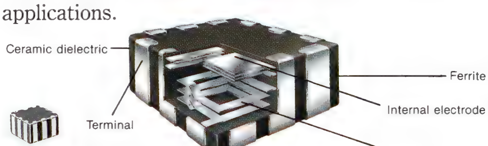
TDK created the world's first inductor without windings by using alternating layers of ferrite paste and conductive silver paste. The unique properties of TDK ferrite give a monolithic closed magnetic circuit with excellent shielding properties, for suitability in high-density configurations. A whole series of multilayer chip inductors are available, starting with the smallest 2012 series. They measure only 2.0 × 1.25 × 0.6 to 1.25mm (.079 × .049 × .024 to .049 inches).



MLF2012 L: 0.047 ~ 33μH **MLF3225** L: 39 ~ 220μH
MLF3216 L: 0.047 ~ 33μH

Multilayer Chip LC Filter

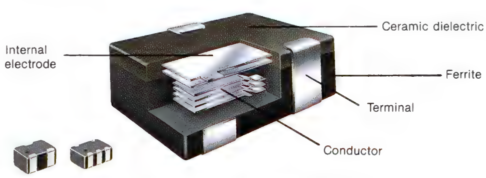
TDK's multilayer technology and simultaneous sintering of magnetic materials and ceramic dielectric materials have created this advanced chip LC filter. An inductor, transformer, and capacitor are layered and integrated into a single monolithic chip measuring only 5 × 5 × 2.8mm (.197 × .197 × .110 inches). This closed magnetic circuit eliminates cross talk and makes this chip ideal for high-density mounting applications.



MXF3535H, B, L, D
MXF4532H, B
MXF5050H, B, L, D
HPF, BPF, LPF, Delay Line

Multilayer Chip LC Trap
Multilayer Chip IF Transformer

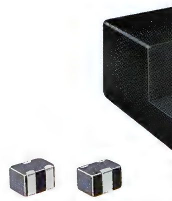
This Multilayer Chip LC Trap and Multilayer Chip IFT feature new chip construction obtained by the simultaneous sintering of different materials, such as ferrite and conductive and ceramic dielectric. Both house closed monolithic magnetic circuits which eliminate cross talk. Their compact size is ideal for high density mounting.



MXT4532 **MIA4532** F: 455kHz
MXT5050 **MIF4532** F: 10.7MHz
F: f₀ ± 3%
F range: 700kHz ~ 10MHz

Multilayer Ch

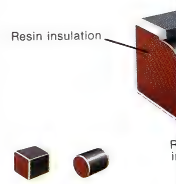
This innovative ch
windings, thanks t
materials, conduct
technology. The t
monolithic design,



MTT4532 L: 10 ~ 200μH

Micro Chip In

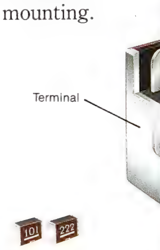
This chip inducto
miniature size wit
Its proprietary clo
insures full magne
ideal for high-densi
low DC resistance



ACL3225S
ACL3225R
L: 0.01 ~ 1,000μH

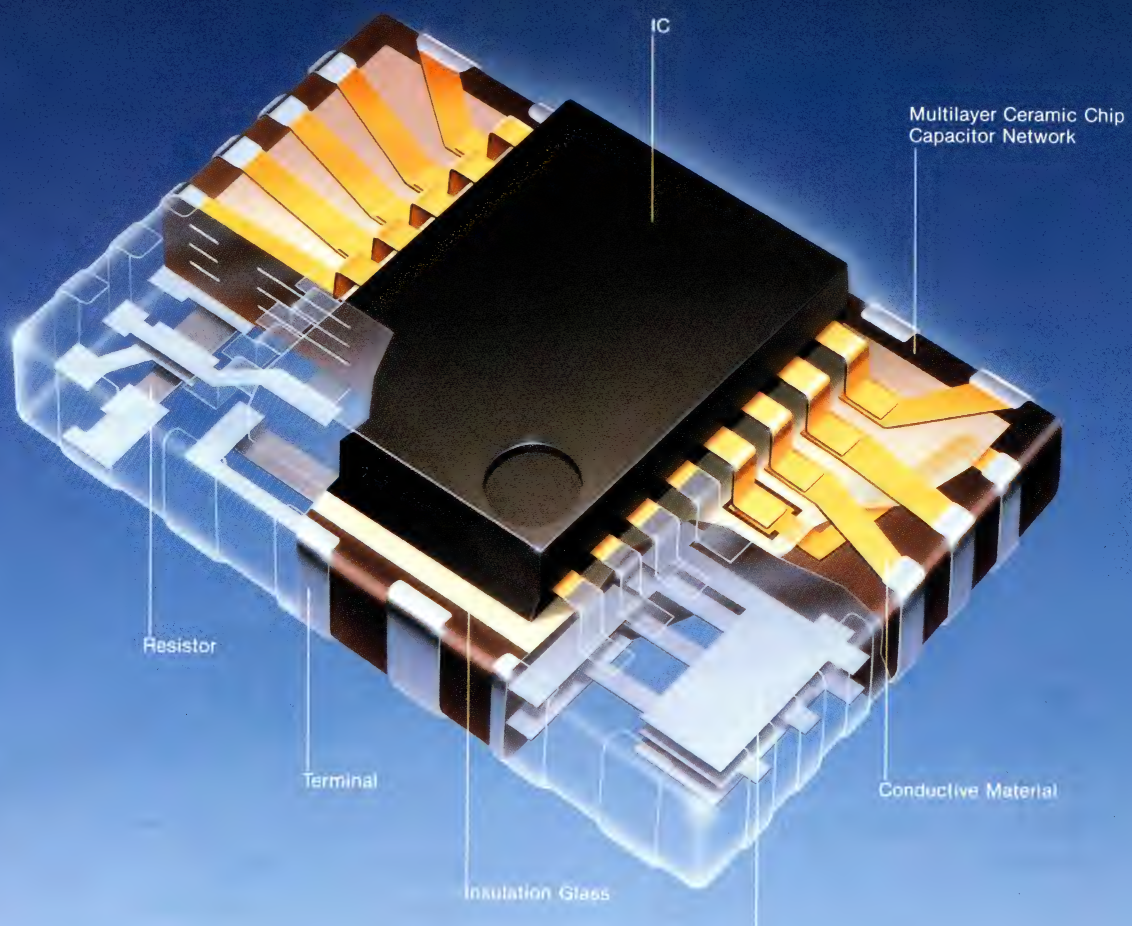
Micro Chip F

This Micro Chip
combination of fer
chip capacitor. Ea
25dB in the 4.5 to
its compact ferrit
excellent magneti
In addition, becau
ACF Series, is on
matches IC pin p
high density
mounting.



ACF453218
Attenuation: 25dB min.
F range: 4.5 ~ 650MHz

TDK's Commitment To Total SMT Gives
For Today's Competitive Marketplaces



TDK Multilayer Hybrid Circuit

TDK TOTAL SURFACE MOUNT TECHNOLOGY

You Unsurpassed Technology

With the pressures to make products smaller, thinner and more reliable, you need a versatile SMT partner...that's TDK. Our Total SMT includes the development of new materials, advanced multilayer SMDs, and sophisticated mounting systems. No one else gives you this level of expertise and support.

New Materials Development For A Solid SMD Foundation

The basis for all SMD product development is R&D in new materials and control, on the microscopic level, of individual crystals. TDK is one of the few firms having experience at the atomic level with these ultra-micron structures. Our expertise encompasses magnetic materials, ceramic dielectric materials, resistive materials and conductive materials. Raw materials are also the basis for total quality control—insuring you that quality is designed in from the start and not added on later.

Advanced Multilayer Chip Devices For Performance, Reliability, and Added Value

TDK's advanced techniques in circuit design and multilayer and composite structures have opened the door to functional modules: single SMD chips containing complete circuit blocks. They handle more efficiently than super-miniaturized discrete components, and are ideal for the high density, high value-added circuit engineering of today and tomorrow. TDK has developed proprietary techniques for fine thick film printing, using many layers of magnetic pastes, ceramic dielectric pastes, and conductive pastes. Our multilayering processes create as many as 90 alternating layers in a single structure.

Simultaneous sintering technology of different materials gives us total control over material behavior for highly predictable results. TDK was the first to succeed in simultaneous sintering of ferrite below 1,000°C (1832°F)—a temperature formerly considered impossible—and apply it to multilayer SMDs with silver conductors. With these techniques, TDK overcame problems such as cracking, peeling, and distortion with mutual diffusion between layers—difficulties previously encountered in simultaneous sintering of different materials.

TDK composite multilayer chip components made with this method feature closed magnetic circuits for excellent magnetic shielding. The low flux leakage avoids crosstalk with other components, permitting extremely high mounting densities.

TDK multilayer SMD chips integrate complete circuit modules, greatly reducing the number of parts and solder connections, simplifying handling, and significantly improving reliability. This means you can create more compact designs with fewer parts, and achieve higher reliability and greater added value.

Sophisticated Mounting Systems For Automation Flexibility

There's no company more qualified to develop surface mounting equipment than TDK...a company with unparalleled experience in surface mount technology. Our AVIMOUNT® series is the third part of our Total SMT commitment, providing you with a complete line-up of automatic mounters, satellite computers, and ancillary equipment for mounting chip components and flat package ICs.

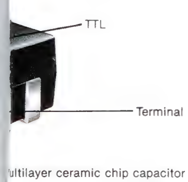
Their most outstanding feature is "Sequencing." This fixes the chip supply system with a programmable pick-and-place machine to select the right parts at the right time. In addition, systems using high-resolution vision cameras detect and correct skewed positions, bent leads, planarity, and the fiducial marks on the PC boards, for high mounting speed and precision.

To achieve the greatest automation flexibility, the AVIC-7800EX satellite computer can control a complete, multi-machine, in-line plant.

TDK's commitment to SMT is as integrated as it is comprehensive: from advanced raw materials to revolutionary multilayer components, to complete turnkey mounting systems. For this most important of today's technologies, make TDK your most important partner.

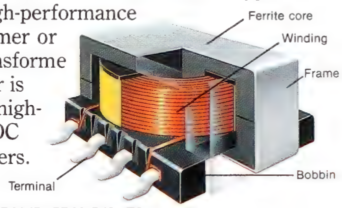
Performance.

ıy Line is of a
: and incorporate
of original TDK
comprised of a chip
chip capactior.
able compact unit.



SM Transformer/Inductor

TDK's highly miniaturized transformer/inductor is designed for today's high-density surface mount applications. The component features two distinct cores: one high-permeability ferrite core, and one low-loss ferrite core with high saturation magnetic flux density. The former is well-suited for applications requiring a high-performance pulse transformer or wide-band transforme while the latter is optimized for high-performance DC to DC converters.

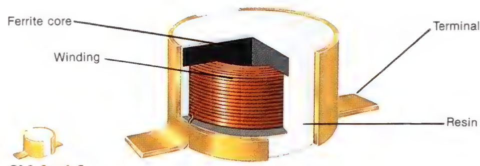


EE5, EE12, ER9.5, ER11/5, ER14.5/6, T2

SM Step-up Inductor

(For Unimorph Piezoelectric Buzzer)

This miniature step-up inductor features high inductance, and works with the unimorph piezo-electric buzzer circuit to produce high sound pressure levels. The inductor is compatible with fully automatic mounting systems.



OL3.3×1.6
OL3.3×2.1

nt CX-5A CX-5230NS CX-5030F / CX-5 CX-5030DD CX-5030DV

Automatic Chip Component Mounter

is ideal for upgrading line capability according to the
flexible, the CX-5230NS has 10 nozzles to mount 8-32mm
5030F has five nozzles to mount odd shaped components.
X-5030DV have two mounting heads. These machines
ax.) of 8-32mm tape widths. The CX-5030DD, equipped
nents
DV,
y

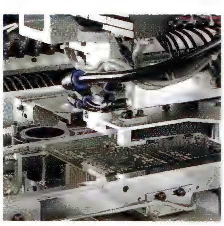
	Mountable component types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
	30 types	0.65 sec.	Max. 457L×356W (17.99L×14.02W) Min. 90L×60W (3.54L×2.36W)	1180L×1160W×1573H (46.46L×45.67W×61.93H)
	15 types	1.1 sec.		
	30 types	1.2 sec.		
	30 types	3.3 sec.		

nt CX-6 CX-6160

Automatic Chip Component Mounter

NEW

self, two mounting
he AVIMOUNT CX-6
000 components/hr.
zles and the unit
pes of components—
components.
plished by simple
ous manufacturing of
mponent changeover.
the system
ons components, thereby assuring high mounting precision.



ountable nent types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
0 types	0.3 sec.	Max. 457L×356W (17.99L×14.02W) Min. 90L×60W (3.54L×2.36W)	2980L×1430W×1548H (117.32L×56.30W×60.94H)

AVIC-7800EX

Satellite Computer System

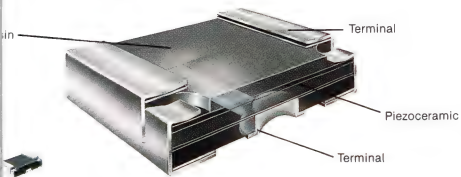
The AVIC-7800EX satellite computer system can control up to eight AVIMOUNT machines. When you put an AVIC-7800EX in your production line, you get equal load capacities since program instructions are dispensed in a well-balanced manner.

FUNCTIONS
1) DNC communications 2) Achievement and schedule management 3) Sequential manufacturing line management 4) Machine control 5) NC Program management 6) Automatic program generation for respective machines 7) Program compiling and editing for respective machines 8) Communication with the host computer in TDK standard format

g Edge Technology For Advanced

eramic Chip Filter • 10.7MHz

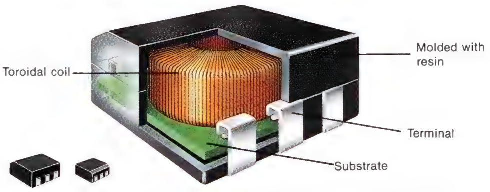
›mpact TDK 10.7MHz Ceramic Chip Filter for
/I tuners is perfect for automatic mounting
4×3.3×1.2mm—.25×.13×.05 inch). Its original
psulated metal terminals allow for excellent
lderability and prevent silver migration.



F1070
10.7±0.03～±0.12MHz

SM Pulse Transformer

This surface mount pulse transformer achieves miniaturization through advanced winding technology and a small, high performance toroidal ferrite core. Its high level of reliability makes it ideal for signal transmission applications.

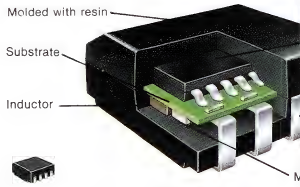


CPT6×6 L: 10～100μH
Winding ratio N1:N2; 1:1

CPT10×10 L: 100～1,000μH
Winding ratio N1:N2:N3; 1:1:1

SM Active Delay Line

This Surface Mount Active Del
5 output lumped constant natur
Fast TTL elements. A product
design, each active delay line is
inductor and multilayer ceramic
Together they form a highly rel



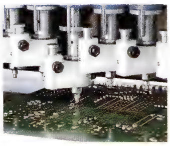
SAD Delay Time: 20～250nsec.

ystematization - TDK Automated Mounting Technology

avimount RX-4A

RX-4260
Automatic Chip Component Mounter

ıe AVIMOUNT RX-4260 high-speed mounting
stem is ideally suited to factory automation
quirements. It features a rotary disk head—an
dustry first. In addition, the RX-4260 has a
quential supply system for easy batch changeover
d for communication with the system's host
mputer. And, since the RX-4260 is a core machine, it can link with
her types of machines for increased component mounting capacity.
or example, an RX-4260 linked to a CX-5030 mounter can handle up to
) different types of components.



Model	Component supply	Mountable component types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
RX-4260	8, 12mm taping	60 types	0.29 sec.	Max. 381L×305W (15.00L×12.01W) Min. 150L×100W (5.91L×3.94W)	2460L×2200W×1600H (96.85L×86.61W×62.99H)

avimou

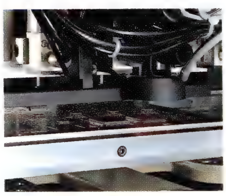
The AVIMOUNT CX-5 Series
manufacturing scale. Compact and
taping components and the CX-
Both the CX-5030DD and the C
mount 30 types of components (m
with a dispenser, mounts compo
onto solder paste. The CX-5030
equipped with vision cameras,
precisely mounts components b
utilizing image processing.

Model	Component supply
CX-5230NS	8～32mm taping
CX-5030F	16～32mm taping, stick
CX-5030DD	8～32mm taping
CX-5030DV	8～32mm taping, stick, tray

avimount CX-4A

CX-4240
IC Mounter with Vision Cameras

he AVIMOUNT CX-4240 is a special-purpose mounting
ystem designed for extremely high mounting precision.
system with two high-resolution vision cameras detects and
›rrects skewed positions, bent leads and planerity, and
ducial marks on the PC boards. Any problems are quickly
›rrected, for high levels of precision and accuracy. The
X-4240 handles flat package ICs, and can accommodate
› to 40 types of SOPs, QFPs, PLCCs, and LCCs. The
-nozzle design enables the mounting of three ICs in a single
peration, with speeds as fast as 2.5 seconds per component.



Model	Component supply	Mountable component types	Speed per component	PC Board dimensions mm (inches)	Unit dimensions mm (inches)
CX-4240	12～36mm taping, TAPE PAK®, MSPAKs	40 types	2.5 sec.	Max. 508L×457W (20.00L×17.99W) Min. 90L×60W (3.54L×2.36W)	1800L×1410W×1590H (70.87L×55.51W×62.60H)

avimou

A complete FMS package in its
heads and one sequence head let t
realize a mounting speed of 12,
Each mounting head has 20 noz
can handle a maximum of 160 t
from micro chips to odd shaped
Lot changeover is easily accom
programming, allowing continu
various types of PCBs without co
Equipped with a vision camera,
automatically centers and positi

Model	Component supply	Mc compo
CX-6160	8～32mm taping, stick	16

TDK SMDs at a glance

TDK

Product name

Type	Shape	Dimensions (mm) [inches] L	W	T

Multilayer Ceramic Chip Capacitor

Type	Shape	L	W	T
C1608 (CC0603)	(EIA Style)	1.6 [.063]	0.8 [.031]	0.9 [.035] max.
C2012 (CC0805)		2.0 [.079]	1.25 [.049]	0.6 [.024]
				0.85 [.033]
				1.25 [.049]
C3216 (CC1206)		3.2 [.126]	1.6 [.063]	0.6 [.024]
				0.85 [.033]
				1.1 [.043]
C3225 (CC1210)		3.2 [.126]	2.5 [.098]	1.9 [.075] max.
C4532 (CC1812)		4.5 [.177]	3.2 [.126]	1.9 [.075] max.
C5650 (CC2220)		5.6 [.220]	5.0 [.197]	1.9 [.075] max.

Large-Capacitance Multilayer Ceramic Chip Capacitor

Type	Shape	L	W	T
HC8050		8.0 [.315]	5.0 [.197]	6.0 [.236]
HC1063		10.0 [.394]	6.3 [.248]	6.0 [.236]
HC1280		12.5 [.492]	8.0 [.315]	6.0 [.236]
HC1612		16.0 [.630]	12.5 [.492]	6.0 [.236]

Mulitilayer Ceramic Chip Capacitor Network

Type	Shape	L	W	T
MCN7575		7.5 [.295]	7.5 [.295]	0.9 [.035]

Multilayer Chip Inductor

Type	Shape	L	W	T
MLF2012		2.0 [.079]	1.25 [.049]	0.85 [.033]
		2.0 [.079]	1.25 [.049]	1.25 [.049]
MLF3216		3.2 [.126]	1.6 [.063]	0.6 [.024]
		3.2 [.126]	1.6 [.063]	1.1 [.043]
MLF3225		3.2 [.126]	2.5 [.098]	1.1 [.043]
		3.2 [.126]	2.5 [.098]	2.5 [.098]

Multilayer Chip LC Filter

Type		Shape	L	W	T
MXF3535L	LPF		3.5 [.138]	3.5 [.138]	2.3 [.091]
			3.5 [.138]	3.5 [.138]	2.8 [.110]
MXF5050L			5.0 [.197]	5.0 [.197]	2.3 [.091]
			5.0 [.197]	5.0 [.197]	2.8 [.110]
MXF3535B	BPF		3.5 [.138]	3.5 [.138]	2.3 [.091]
			3.5 [.138]	3.5 [.138]	2.8 [.110]
MXF5050B			5.0 [.197]	5.0 [.197]	2.3 [.091]
			5.0 [.197]	5.0 [.197]	2.8 [.110]
MXF3535H	HPF		3.5 [.138]	3.5 [.138]	2.3 [.091]
			3.5 [.138]	3.5 [.138]	2.8 [.110]
MXF5050H			5.0 [.197]	5.0 [.197]	2.3 [.091]
MXF3535D	Delay Line		3.5 [.138]	3.5 [.138]	2.3 [.091]
			3.5 [.138]	3.5 [.138]	2.8 [.110]
MXF5050D			5.0 [.197]	5.0 [.197]	2.3 [.091]
			5.0 [.197]	5.0 [.197]	2.8 [.110]
MXF4532B	BPF (FM)		4.5 [.177]	3.2 [.126]	2.2 [.087]
MXF4532H	HPF (TV)		4.5 [.177]	3.2 [.126]	1.6 [.063]

Multilayer Chip LC Trap

Type	Shape	L	W	T
MXT4532		4.5 [.177]	3.2 [.126]	2.2 [.087]
		4.5 [.177]	3.2 [.126]	2.8 [.110]
		4.5 [.177]	3.2 [.126]	3.0 [.118]
MXT5050		5.0 [.197]	5.0 [.197]	2.3 [.091]

Multilayer Chip IF Transformer

Type	Shape	L	W	T
MIA4532 (AM radio)		4.5 [.177]	3.2 [.126]	2.8 [.110]
MIF4532 (FM radio)		4.5 [.177]	3.2 [.126]	2.2 [.087]

Multilayer Chip Transformer

Type	Shape	L	W	T
MTT4532		4.5 [.177]	3.2 [.126]	2.8 [.110] max.
MTT5050		5.0 [.197]	5.0 [.197]	2.3 [.091] max.

Micro Chip Inductor (Wound Micro Chip Inductor)

Type	Shape	L	W	T
ACL3225S		3.2 [.126]	2.5 [.098]	2.5 [.098]
ACL3225R		3.2 [.126]	⌀2.5 [.098]	—

Product name

Micro Chip EMI Filter

Type	Shape	L	W	T
ACF453218		4.5 [.177]	3.2 [.090]	1.8 [.071]

Leadless Inductor (Wound Chip Inductor)

Type	Shape	L	W	T
NL322522		3.2 [.126]	2.5 [.098]	2.2 [.087]
NL453232		4.5 [.177]	3.2 [.126]	3.2 [.126]
NL565050		5.6 [.220]	5.0 [.197]	5.0 [.197]
NLF453232		4.5 [.177]	3.2 [.126]	3.2 [.126]

Power-Line Leadless Inductor (Wound Chip Inductor)

Type	Shape	L	W	T
NLC322522		3.2 [.126]	2.5 [.098]	2.2 [.087]
NLC453232		4.5 [.177]	3.2 [.126]	3.2 [.126]
NLC565050		5.6 [.220]	5.0 [.197]	5.0 [.197]

Leadless Line Choke SF Coil (Wound Chip Line Choke)

Type	Shape	L	W	T
SFMR820		8.5 [.335]	7.5 [.295]	6.0 [.236]
SFM0520				
SFM1010				

Leadless LC Trap (Wound Chip LC Trap)

Type	Shape	L	W	T
NLT4532		4.5 [.177]	3.2 [.126]	3.2 [.126)

Leadless EMI Filter (Wound Chip EMI Filter)

Type	Shape	L	W	T
NLL4532		4.5 [.177]	3.2 [.126]	3.2 [.126]

Ferrite Chip EMI Suppressor

Type	Shape	L	W	T
CB201209		2.0 [.079]	1.25 [.049]	0.9 [.035]
CB321611		3.2 [.126]	1.6 [.063]	1.1 [.043]
CB322513		3.2 [.126]	2.5 [.098]	1.3 [.051]
CB453215		4.5 [.177]	3.2 [.126]	1.5 [.059]

NTC Chip Thermistor

Type	Shape	L	W	T
NTCCS2012		2.0 [.079]	1.25 [.049]	0.9 [.035] max.
NTCCS3216		3.2 [.126]	1.6 [.063]	1.3 [.051] max.

Ceramic Chip Filter·10.7MHz

Type	Shape	L	W	T
CEF1070MA		6.4 [.252]	3.3 [.130]	1.2 [.047]
CEF1070NA				
CEF1070MS				

SM Pulse Transformer

Type	Shape	L	W	T
CPT6×6		6.9 [.271]	6.5 [.255]	4.6 [.181]
CPT10×10		10.8 [.425]	10.5 [413]	5.2 [.205]

SM Active Delay Line

Type	Shape	L	W	T
SAD020		12.6 [.496]	11.6 [.457]	4.7 [.185]
SAD025				
SAD050				
SAD060				
SAD075				
SAD100				
SAD125				
SAD150				
SAD200				
SAD250				

SM Transformer/Inductor

Type	Shape	L	W	T
EE5		8.2 [.323] max.	6.5 [.256] max.	5.2 [.205] max.
EE12/5/6		14.0 [.551] max.	12.8 [.504] max.	6.5 [.256] max.
ER9.5/5		12.5 [.492] max.	10.7 [.421] max.	5.7 [.224] max.
ER11/5		13.0 [.512] max.	12.0 [.472] max.	6.3 [.248] max.
ER14.5/6		17.2 [.677] max.	15.5 [.610] max.	7.2 [.283] max.
T2		8.0 [.315] max.	5.5 [.217] max.	2.5 [.098] max.

SM Step-up Inductor (Unimorph Piezoelectric Buzzer)

Type	Shape	L	W	T
OL3.3×1.6		5.4 [.213]	3.3 [.130]	1.6 [0.63]
OL3.3×2.1		5.4 [.213]	3.3 [.130]	2.1 [.083]

To receive a copy of TDK's SMT catalog, containing all SMDs and AVIMOUNT® systems, contact the TDK office nearest you.

TDK CORPORATION OF AMERICA HEAD OFFICE 1600 Feehanville Drive, Mount Prospect, IL 60056, U.S.A. Phone: (312) 803-6100 CHICAGO REGIONAL OFFICE Phone: (312) 803-6100 INDIANAPOLIS REGIONAL OFFICE Phone: (317) 872-0370 NEW YORK REGIONAL OFFICE Phone: (516) 625-0151 LOS ANGELES REGIONAL OFFICE Phone: (213) 539-6631 DETROIT DISTRICT OFFICE Phone: (313) 353-9393 NEW JERSEY DISTRICT OFFICE Phone: (201) 736-0023 BOSTON DISTRICT OFFICE Phone: (508) 624-4262 HUNTSVILLE DISTRICT OFFICE Phone: (205) 464-0222 GREENSBORO DISTRICT OFFICE Phone: (919) 292-0012 DALLAS DISTRICT OFFICE Phone: (214) 506-9800 SAN FRANCISCO DISTRICT OFFICE Phone: (408) 437-9585 **TDK ELECTRONICS EUROPE GmbH.** HEAD OFFICE Christinenstrasse 25, D-4030 Ratingen 1, F.R. Germany Tel.: (02102) 4870 RATINGEN OFFICE Harkortstrasse 6, D-4030 Ratingen 1, F.R. Germany Tel.: (02102) 4870 STUTTGART OFFICE Tel.: 0711-780560 PARIS LIAISON OFFICE Tel.: 1-46.02.71.65 MILANO LIAISON OFFICE Tel.: 02-98240776 **TDK U.K. LIMITED** COMPONENTS DEPARTMENT TDK House 5-7 Queensway Redhill, Surrey RH1 1YB United Kingdom Tel.: 0737-772323 **TDK CORPORATION** KOREA BRANCH Phone: Seoul (02) 554-6633 **TDK CORPORATION** BEIJING REPRESENTATIVE OFFICE Phone: (01) 512-3111 **TDK TAIWAN CORPORATION** TAIPEI Phone: (02) 712-5090 **TDK HONG KONG CO., LTD.** Phone: 3-7362238 **TDK SINGAPORE (PTE) LTD.** Phone: 2735022 **TDK DO BRASIL IND. E COM. LTDA.** Phone: 289-9599 **TDK CORPORATION** 13-1, Nihonbashi 1-chome, Chuo-ku, Tokyo 103, Japan Phone: Tokyo (03) 278-5111

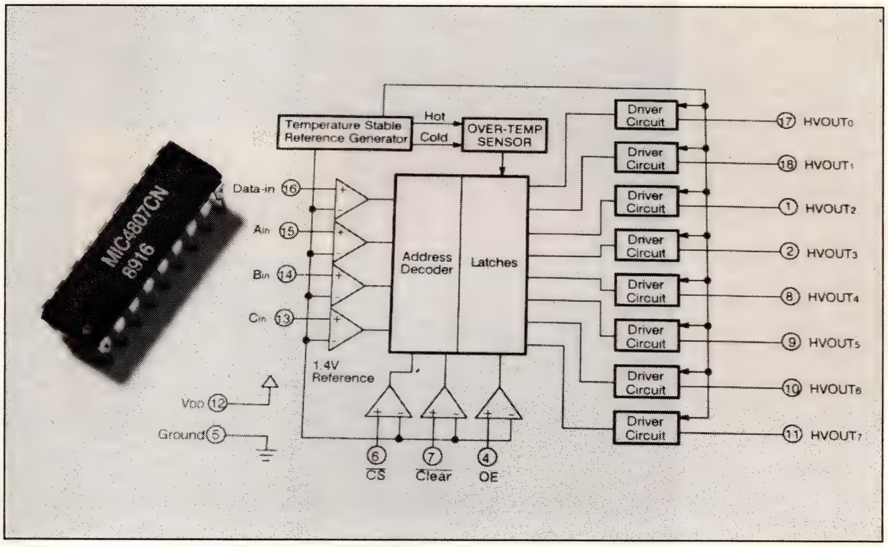
NEW PRODUCTS

INTEGRATED CIRCUITS

8-CHANNEL DRIVER

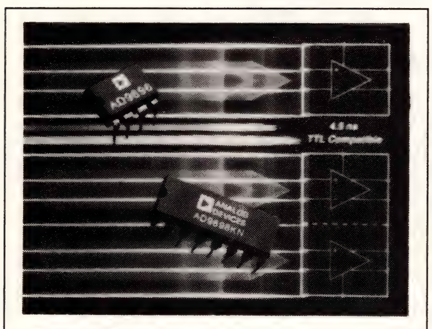
- *Features 80V-rated outputs*
- *Contains address decoder and latches*

Containing a number of improvements over earlier versions of this type of device, the MIC4807 8-channel driver is pin compatible with the Sprague UCN4807 and a direct replacement in most applications. The MIC4807 operates as high as 100V, draws only 10 mA of supply current, doesn't need a 5V base-drive supply, and functions in a failure mode to 80V. The MIC4807 also features a built-in current limiter that holds the sink current to 200 mA in the event of a short circuit to the positive supply, and an over-temperature sensor that shuts down all the outputs when the chip temperature exceeds 145°C. The sensor circuit restores operation at 45°C. Logic inputs are TTL and CMOS compatible. The MIC4807 comes in an 18-pin plastic DIP. $3.95 (100). Delivery, stock to 45 days ARO.



Micrel Inc, 560 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 245-2500. FAX 408-245-4175. TWX 910-379-0007.

Circle No 394



FAST COMPARATORS

- *Have 4.5-nsec propagation delay*
- *Single and dual versions available*

The single AD9696 and dual AD9698 TTL-compatible comparators feature a typical propagation delay of 4.5 nsec (7 nsec max). The devices, which are suitable for high-speed communications and automatic-test-equipment applications, also feature an offset voltage of 2 mV max and a 1.7-nsec setup time. Both devices are configurable for two input-voltage ranges. Using a single 5V supply, the comparator's input range is 1.4 to 3.7V. Using a dual ±5V supply, the input range extends from 2.2 to 3.7V. The dual AD9698 is particularly useful in applications that require close matching between units. The comparators are available in commercial- and military-temperature grades. The AD9696 is packaged in 10-pin TO-100 metal cans, 8-pin ceramic DIPs, or 8-pin SOICs. The AD9698 is packaged in either 16-pin ceramic or plastic DIPs, or 16-pin SOICs. AD9696, $3.50; AD9698, from $6 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (919) 668-9511.

Circle No 395

POWER OP AMP

- *Operates from supplies to ±35V*
- *Has a 5A (10A pk) output rating*

Packaged in an 11-pin high-power plastic package, the OPA541AP power op amp features a ±35V supply rating and a continuous output-current rating of 5A (10A pk). The open-loop gain at 10 Hz is 97 dB typ (90 dB min), and the small-signal bandwidth is 1.6 MHz. The plastic package, which has a copper lead frame to maximize heat transfer, has a junction-to-case thermal resistance of 2.5°C/W at a 60-Hz output. With no heat sink, the junction-to-ambient thermal resistance is 40°C/W. From $9.95 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX 602-889-1510.

Circle No 396

AUDIO PROCESSOR

- *Contains multiple functions*
- *Features a 100-dB dynamic range*

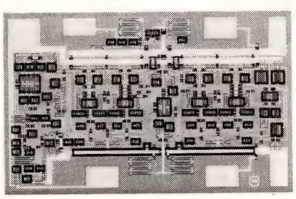
Called a Dynamic Range Processor, the SSM-2120 combines multiple signal- processing functions in a single monolithic chip. Packaged in a 22-pin DIP, the SSM-2120 permits full access to its two voltage-controlled amplifiers and level detectors. Depending on the connection

NOW PUT A LITTLE AVANTEK MAGIC IN YOUR SYSTEM

Avantek MagIC™ High Speed ICs Enable Superior System Designs

magIC™

The new MagIC™ series of silicon bipolar MSI integrated circuits offer the best performance available from silicon ICs yet. The broadband, high frequency performance of these high-speed silicon ICs make them cost-effective alternatives to more expensive GaAs ICs. Avantek MagIC silicon ICs are manufactured with Avantek's proprietary 10-15 GHz F_t, 25 GHz F_{max} Isosat™ process for unsurpassed integration and performance at microwave frequencies. Avantek's MagIC series ICs presently consists of four product families: low noise amplifiers, active mixers, variable gain control amplifiers, and prescalers. These low-cost, high-speed silicon ICs are Avantek's magic solutions to your RF, microwave and lightwave system performance and cost problems.



High Performance, High Speed, Low Cost...

The INA-series of two-stage low-noise amplifiers presently consists of three models, offering:
- 3 dB bandwidths to 2.8 GHz
- Gains as high as 32 dB
- Noise figures as low as 1.7 dB
- Prices as low as $22.00 each* in hermetic 70 mil surface mount package

The IAM-series of active mixer/amplifiers presently consists of two models, offering:
- RF and LO frequency range of .05 to 5.0 GHz
- Conversion gain as high as 15 dB
- LO power as low as −10 dBm
- Prices as low as $16.00 each* in hermetic 180 mil surface mount package

The IVA-series of variable gain control amplifiers presently consists of two models, offering:
- 3 dB bandwidths to 3.0 GHz
- 30 dB gain control range
- Gains as high as 26 dB
- Prices as low as $28.50 each* in hermetic 180 mil surface mount package

The IFD-series low phase noise static prescalers offer:
- Divide-by-4 to 5 GHz
- Low 125 mW Power Consumption
- Prices as low as $18.50 each* in hermetic 100 mil surface mount package

*Price for 1000 piece quantities

MagIC™ ICs Are Available in Quantity for Volume Applications

Avantek presently produces more than 1,000,000 MMICs per month. So you can be assured the MagIC high speed ICs you need will be available to support your volume production programs. And, all MagIC silicon ICs are in stock at your local Avantek distributor.

For additional information, or the name and address of your local distributor, contact the regional sales office nearest you.

Regional Sales Offices
North America
Eastern: (301) 381-2600
Central: (312) 358-8963
Western: (805) 373-3870
European: (44) 276-685753

Magic Solutions in Silicon

AVANTEK

CIRCLE NO 186

of external components, the chip can perform numerous dynamic-range processing functions such as companding, automatic gain control, compression, peak limiting, and noise gating. The chip's class-A amplifiers offer a dynamic range of 100 dB with 0.01% THD. The SSM-2120 operates from a 5 to 18V supply. $4.15 (100).

Precision Monolithics, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX 408-727-1550.

Circle No 397

12-BIT ADC

- *Self-calibrating*
- *Includes S/H circuit*

The ADC1241 12-bit, +sign A/D converter combines a self-calibration capability with an on-chip S/H circuit. The self-calibration feature includes autozero capability during every conversion and corrects zero- and full-scale errors to $<\pm 1$ LSB and linearity errors to $\pm\frac{1}{2}$ LSB. The ADC1241 has a maximum conversion time of 13.8 μsec and is guaranteed to have no missing codes over its operating-temperature range. The ADC uses successive-approximation conversion and has an analog-input voltage range of 0 to 5V (unipolar) or -5 to $+5$V (bipolar). The digital output is 2's complement in a 13-bit parallel word. The μP interface is compatible with high-speed processors, and input/output lines are compatible with TTL and CMOS logic. The ADC1241 uses an external 5V reference and operates from a ±5V supply. 28-pin ceramic DIP, $15.90 (100).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2273. TLX 346353.

Circle No 398

MICROPROCESSOR

- *3-chip set*
- *Optimized for real-time operations*

The MAS281 μP is a MIL-STD-1750A, 16-bit CPU that consists of three chips: the MA17501 execution unit, the MA17502 control unit, and the MA17503 interrupt unit. These three units are mounted and interconnected on a 64-pin dual-in-line ceramic substrate. The MAS281 is optimized for real-time I/O and arithemetic-intensive operations and supports a 64k-word address space. You can add the optional MA17504 memory-management chip to expand the address space to 1M words. Key features include a parallel multiplier/accumulator, a 32-bit barrel shifter, an instruction prefetch queue, and a multiport register file. Other features include built-in test capability, A and B interval timers, and a start-up ROM

Some designers already take enclosures very seriously.

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The comprehensive Rittal Handbook. It's easy to get, and it's free. Just give us a call and we'll tell you how you can take your designs all the way to perfection . . . with enclosure systems from Rittal.

1-800-637-4425

RITTAL Corporation, 3100 Upper Valley Pike, P.O. Box 1284, Springfield, Ohio 45504, Tel: (513) 399-0500, Fax: (513) 390-5599
CANADA, RITTAL LTD., P.O. Box 986, Oakville, Ontario L6J5E8, Tel: (416) 338-2440, Fax: (416) 845-5901, Telex: 6968914

interface. Manufactured in a CMOS silicon-on-sapphire process, the MAS281 features low-power and high-speed operation. Prototypes, from $2000.

Marconi Circuit Technology, 45 Davids Dr. Hauppauge, NY 11788. Phone (516) 231-7710.

Circle No 399

QUAD 8-BIT DAC

- *Has four buffer-amplifier outputs*
- *Has a cascadable serial interface*

The MAX500 contains four 8-bit DACs, which feature double-buffered digital inputs and independent voltage outputs through four buffer amplifiers. Compared with a parallel interface, the chip's cascadable 2- or 3-wire serial interface requires fewer package pins and reduces isolation requirements. In the 3-wire serial mode, the MAX500 shifts 10-bit words (2 address bits and 8 data bits) from the serial-data line to an on-chip shift register. On the Load command, the chip transfers its shift-register data to the DAC register indicated by the address. The host processor can shift in three more words to update the remaining registers, and then simultaneously update the converter outputs by strobing Load DAC. The MAX500 works with dual supplies or with a single 12 to 15V supply and is available in 16-pin DIP or SO packages. From $12.60 (100).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 400

I/O CONTROLLERS

- *For PC applications*
- *Contain serial and parallel ports*

Designed for PC I/O applications, the SAB 82C250-N and SAB 82C251-N contain both serial and parallel ports. The 82C250-N integrates two serial I/O ports with a parallel (bidirectional) printer interface. The 82C251-N contains one serial I/O port and one parallel interface. The 82C250-N is pincompatible with the industry's 16C452; the 82C251-N is pin compatible with the 16C451. The devices offer the additional capability of using the parallel port in IBM PS/2 register-compatible mode. The serial output ports are fully compatible with the SAB 16C450. In 68-pin plastic leaded-chip carriers: SAB 82C250-N, $10; SAB 82C251-N, $7 (1000).

Siemens Components Inc, Integrated Circuit Div, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4526.

Circle No 401

Multiply your DSP system performance, not your system cost.

New High-Performance Multipliers At Competitive Prices.

You can improve a cost/performance ratio two ways: lower the cost or boost performance. We're doing both.

Introducing higher-performance multipliers at prices you'd expect from commodity-quality vendors.

These new 16-bit multipliers offer function flexibility and performance fast enough for real-time signal processing and control: 35 ns maximum clocked time to multiply for commercial temperatures. All draw 90% less power than slower bipolar multipliers — 750 mW maximum at rated speed.

And all are compatible with industry standard multiplier functions, pinouts and packages.

Different Configurations Handle Different Needs.

- The **HMU16's** separate clocks simplify bus interfacing.
- The **HMU17's** single clock and separate enables are geared to microprogrammed systems.
- The **HMU18's** dedicated 32-bit output bus accommodates faster I/O applications.

Ask for our brochure and see how our multipliers meet your system price and performance goals.

Contact Harris Semiconductor, Mercure Centre, Rue de la Fusee 100, 1130 Brussels, Belgium. Phone (32) 2-246-2330.

What your vision of the future demands. Today.

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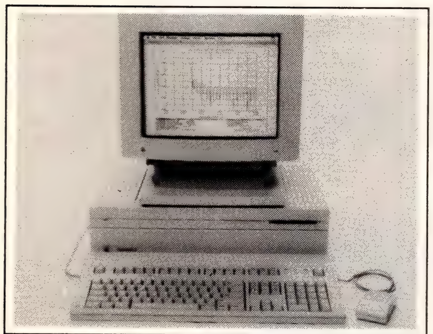
CIRCLE NO 197

CAE & SOFTWARE DEVELOPMENT



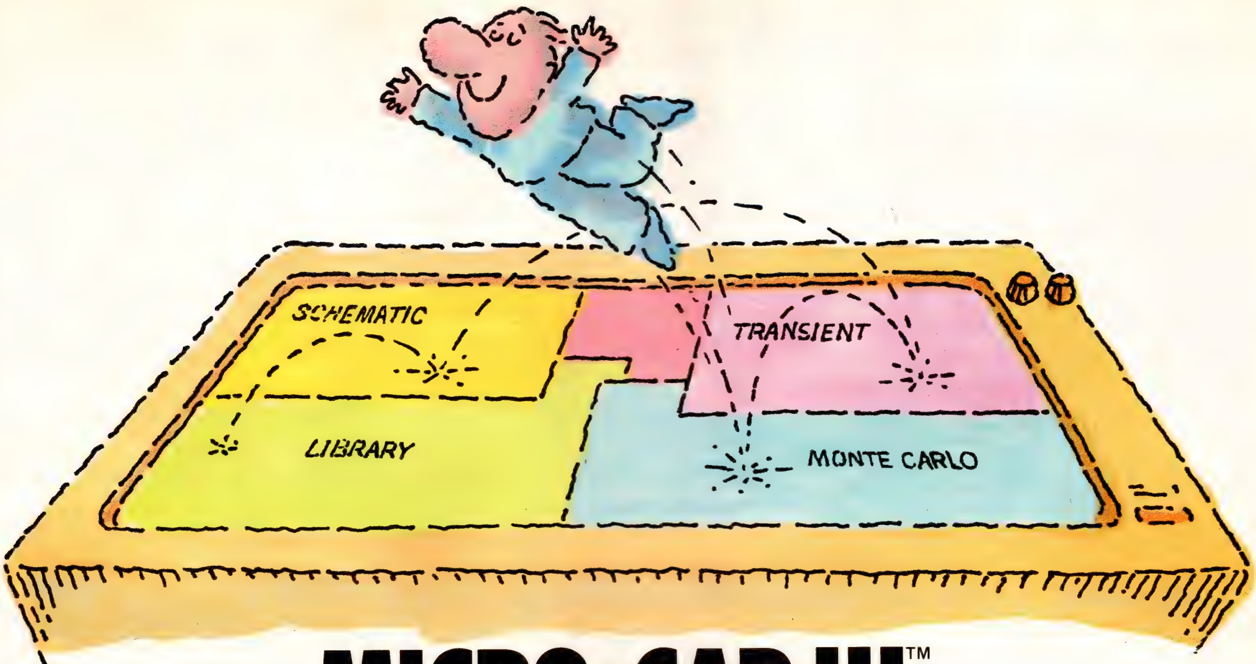
FILTER DESIGNER

- *Handles IIR, FIR, and Parks-McClellan filters*
- *Runs on Macintosh SE and Mac II computers*

MacFilter is a filter-design and -analysis program that runs on Macintosh SE and II computers and is similar to the vendor's FDAS2 package. The program provides extensive error checking and detailed help screens. You can design and analyze three general types of filters: FIR (Finite Impulse Response), IIR (Infinite Impulse Response), and Parks-McClellan Equiripple FIR. The IIR feature lets you design lowpass, highpass, bandpass, and bandstop filters with Butterworth, Chebyshev, elliptic, and Bessel responses and orders as great as 40 for lowpass and highpass and 80 for bandpass and bandstop filters. The IIR feature lets you design differentiator and multiband filters in addition to the FIR types; a filter may have as many as 2048 taps, and you can use rectangular, Hanning, Hamming, triangular, Blackman, or Kaiser window functions. The Parks-McClellan feature lets you design Hilbert transformers and arbitrary-magnitude filters in addition to the IIR types; a filter may have as many as 400 taps. When you have completed your filter specification, you can call up a separate code generator that automatically generates assembly-language source code for the Motorola 56001 processor. To maximize precision and dynamic range, the system uses double-precision (64-bit) floating-point computations. For output to the target processor, however, you can select one of a variety of fixed-point, floating-point, and block-floating-point formats. MacFilter, $995; 56001 code generator, $200.

Momentum Data Systems, 1520 Nutmeg Pl, Suite 108, Costa Mesa, CA 92626. Phone (714) 557-6884. FAX 714-557-6969.

Circle No 390

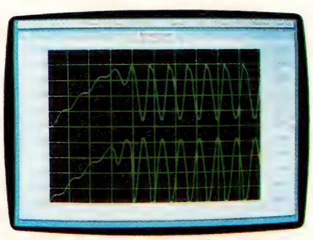


MICRO-CAP III.™ THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

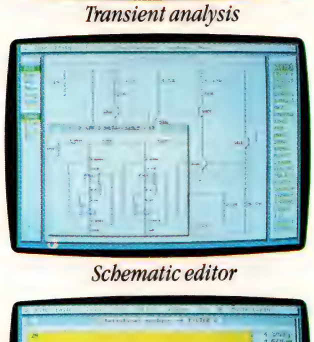
MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

The program's window-based operation and schematic editor make circuit creation a breeze. And super-fast SPICE-like routines mean quick AC, DC, Fourier and transient analysis—right from schematics. You can combine simulations of digital and analog circuits via integrated switch models and macros. And, using stepped component values, rapidly generate multiple plots to fine-tune your circuits.

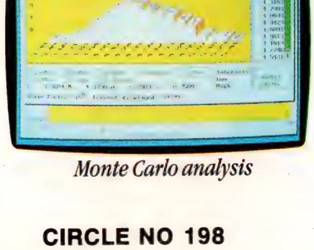
We've added routines for noise, impedance and conductance—even Monte Carlo routines for statistical analysis of production yield. Plus algebraic formula parsers for plotting almost any desired function.



Transient analysis



Schematic editor



Monte Carlo analysis

Modeling power leaps upward as well, to Gummel-Poon BJT and Level 3 MOS—supported, of course, by a built-in Parameter Estimation Program and extended standard parts library.

There's support for Hercules,® CGA, MCGA, EGA and VGA displays. Output for laser plotters and printers. And a lot more.

The cost? Just $1495. Evaluation versions are only $150.

Naturally, you'll want to call or write for a free brochure and demo disk.

spectrum

1021 S. Wolfe Road,
Sunnyvale, CA 94086
(408) 738-4387

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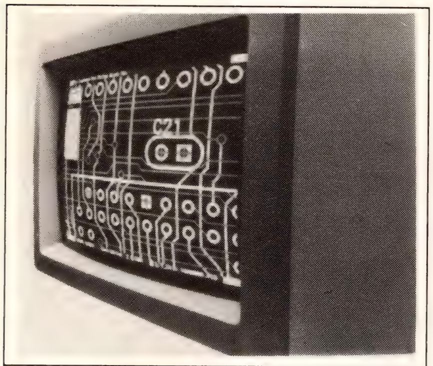
CIRCLE NO 198



ENHANCED EDA TOOLS

- *Permit use of expanded memory for large designs*
- *Provide more than 100 screens of context-sensitive help*

Tango-PCB Plus and Tango-Route Plus are greatly enhanced versions of the vendor's pc-board design and autorouter products for IBM PCs and compatibles. Both electronic-design-automation (EDA) packages now allow you to use as much as 8M bytes of expanded memory with the LIM EMS 3.2 standard or 32M bytes with the LIM EMS 4.0 standard for when you want to work with complex designs that have more than 100 equivalent ICs (the limit imposed by the earlier Tango-PCB and Tango-Route packages). The new design-rule-checking feature checks the board design against an input net list to verify conformance to the user's rules for both connectivity and clearance. A placement-aid feature uses force vectors to show the best board position for each component in relation to all the others; the vectors appear on the screen as arrows that change length and direction as you move a given component—the shorter the arrows, the better the placement. Enhancements to the router include an increase in autorouting capability from two layers to six (plus power and ground planes) and a broader range of routing grids (25, 20, 16.7, 12.5, and 10 mils). The finer grids permit as many as five traces between IC pads. The placement of vias for surface-mount technology designs has also been improved. Tango-PCB Plus and Tango-Route Plus, $895 each; both combined as Tango-CADPak Plus, $1495.

Accel Technologies Inc, 6825 Flanders Dr, San Diego, CA 92121. Phone (619) 554-1000. FAX 619-554-1019.

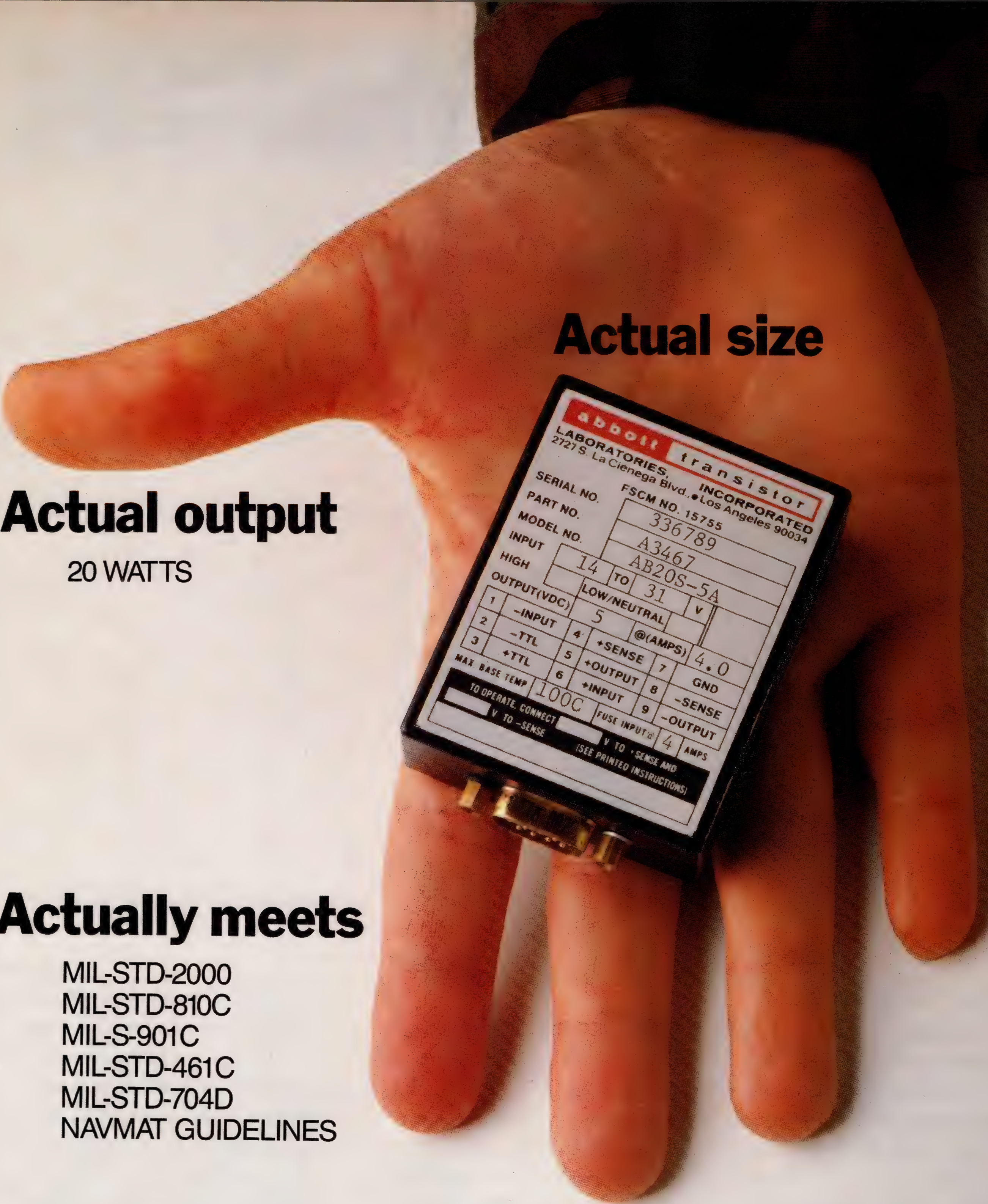
Circle No 391

8051 CROSS-ASSEMBLER

- *Generates object code for 8051 and derivative microcontrollers*
- *Written in 8086 assembly language for speed and reliability*

This cross-assembler, which is written in 8086 assembly language for maximum speed and reliability, runs on any IBM PC or compatible

Actual size



Actual output

20 WATTS

Actually meets

MIL-STD-2000
MIL-STD-810C
MIL-S-901C
MIL-STD-461C
MIL-STD-704D
NAVMAT GUIDELINES

Mil/Pac™ high-density military power supplies. Introducing NDI DC-to-DC converters that meet an unprecedented combination of military design demands. Plus having the highest power-to-volume ratios of any full-mil qualified products.

Mil/Pacs come in 20W, 35W and 50W configurations, with single (5, 12, 15, 24, 28V) and dual (±12V; ±15V) outputs.

They handle a wide 14V to 31V range of input. And operate at temperature extremes from −55°C to +100°C.

Mil/Pacs are designed with a field-proven topology that's been verified by rigorous environmental stress screening. They're available with MIL-STD-2000, or without. Either way, the specs are worth reading.

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WHEN RELIABILITY IS IMPERATIVE.™

CIRCLE NO 200

computer. It accepts 8051 assembly-language source code and generates object code in Intel Hex format for downloading to the target machine; command-line switches let you optionally generate assembly-code listings and symbol-table files. As an aid to programming, the cross-assembler lets you use local labels and include files; symbol names may have as many as 32 significant characters. You can generate code for any 8051 or derivative microcontroller. During assembly, the program keeps you informed of progress. If it finds an error, it emits one of the 25 explicit error messages. $95.

Parallax Inc, 6200 Desimone Lane, Suite 69A, Citrus Heights, CA 95621. Phone (916) 721-8217.

Circle No 392

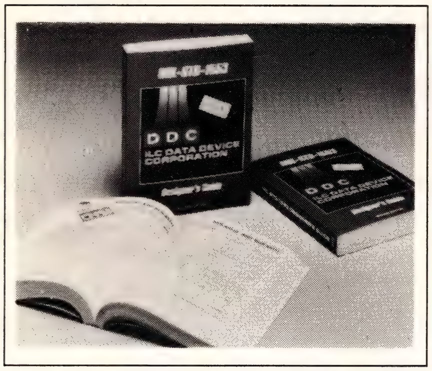
ANALOG SIMULATOR

- *Analyzes linear circuits that have as many as 200 components*
- *Runs on any Macintosh that has at least 512k bytes of memory*

ACNAP (AC Network Analysis Program) is a general-purpose, circuit-simulation program that analyzes linear circuits with as many as 200 active and passive components. The program performs Bode, Monte Carlo, sensitivity, noise-equivalent bandwidth, component-iteration, spectrum, and worst-case analyses. You can create macros of unlimited length, in which you can embed comments, delays, and pauses, in order to automate repetitive tasks or to set up instructional sequences for training purposes. You can create, combine, and edit component models and circuits, and then save them as single devices in a component library. The program allows such user-defined subcircuits to have as many as seven external connections, so that you can easily model and manipulate very complex types of devices. There are built-in drivers for ImageWriter (dot-matrix) and LaserWriter (laser) printers, and you can obtain an optional plotter driver that will drive most popular color-pen plotters. The program runs on any Macintosh computer that has at least 512k bytes of memory and runs System 3.2 or later, or Finder 5.3 or later. ACNAP, $349.95; optional plotter driver, $95.

BV Engineering Professional Software, 2023 Chicago Ave, Suite B-13, Riverside, CA 92507. Phone (714) 781-0252.

Circle No 393



Wide coverage of MIL-STD-1553 products

Aimed at system designers who must meet military requirements, the 604-pg *MIL-STD-1553 Designer's Guide* provides an overview of MIL-STD-1553 and a comparison of several of its variations, as well as system hardware and software considerations. The book also presents a complete copy of MIL-STD-1553B with paragraph-by-paragraph commentaries on the standard and a comparison with the A version. Also included are changes to the original 1553 Standard and copies of the ASD (Avionics Systems Div) Validation Test Plan and the RT (Remote Terminal) Production Test Plan. The data-bus applications section covers guidelines for making MIL-STD-1553 components work with µPs, single-chip microcomputers, and a dual-port RAM. A full listing of application notes, updated product-information sections, and a complete listing of the vendor's MIL-STD-1553 components and board-level products complete the book.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 380

Disk demonstrates universal programmers

Rather than describing its product in a brochure, one company offers a demo disk that shows off the functions of the various Sailor Programmer models. In addition to representing the actual Sailor Programmer software, the disk also serves as a utility for splitting and merging data files, as well as converting binary data files into Intel hex or Motorola data files.

Advin Systems Inc, 1050-L E Duane Ave, Sunnyvale, CA 94086.

Circle No 381

Catalog details coaxial components

The 60-pg Coaxial Components Catalog (Literature 5959-7861) provides specifications and operating and installation information about switches, detectors, and fixed and step attenuators. The publication highlights the HP 33314 spdt coaxial switch, which is specified for a 5M-cycle life having >0.03-dB repeatability. Also featured are the latest 11-, 70-, and 90-dB step attenuators with a range to 40 GHz, as well as several families of coaxial detectors.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014.

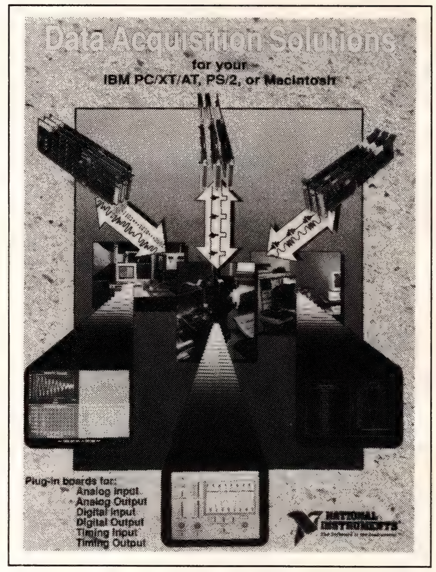
Circle No 382

Reference focuses on STD Bus system development

This 1990 STD Bus system-development guide surveys the company's full range of board-level products, development systems, software, and card cages. Highlighted are PC-compatible modules and systems based on 80386, 80286, 80188, and 8088 processors. Other categories in the 82-pg reference include BitBus interfaces for factory networking, an ample selection of industrial- and analog-I/O boards, and specialized boards for stepper-motor control, video imaging, and other functions. Each section begins with an easy-to-use board-selection guide, and the product listings include specifications, diagrams, and photos. Further, application notes covering a variety of uses for STD Bus products and a list of vendors of complementary computer-system components are included.

Computer Dynamics, 107 S Main St, Greer, SC 29650.

Circle No 383



Foldout depicts PC data-acquisition products

This 6-pg foldout brochure highlights the technical specifications for plug-in data-acquisition boards for the Nubus, the IBM PC/AT bus, the Micro Channel Architecture (MCA) bus, and the Macintosh SE. The publication also discusses the vendor's RTSI (real-time system integration) Bus for precise timing and synchronization between multiple plug-in boards. The brochure describes the company's LabDriver, LabWindows, Measure application software, LabView software, and data-acquisition accessories.

National Instruments, 12109 Technology Blvd, Austin, TX 78727.

Circle No 384

Military DC/DC Converters
+5, +12, ±12, +15, ±15V
Single and dual output

AHE Series DC/DC converters from Advanced Analog have the power and reliability needed for military and aerospace systems.

- -55°C to +125°C and -55°C to +85°C temperature range
- Screened to MIL-STD-883C, Method 5008 in a MIL-STD-1772 certified facility
- 15W and 20W output power
- Hermetically sealed
- Advanced feedback method uses no optocouplers for high reliability and greater radiation tolerance

Now you can get the higher temperature range your system requires. And improved performance. Advanced Analog's AHE Series are built for rugged environments and guaranteed to outperform any other standard DC/DC converter of this type. Other standard Mxx Series converter models are available.

We've got the experience. Our PS Series triple-output, 80W converter is serving in the newest attack helicopter.

Need a special converter or power hybrid? Call us and we'll work with your team to get the best solution for your needs.

DC/DC Converters

	Output Power	Output Voltage (V) Current (A)
AHE2805S	15	5V, 0 - 3A
AHE2812S	20	12V, 0 - 1.67A
AHE2812D	15	±12V, 0 - 625mA
AHE2815S	20	15V, 0 - 1.33A
AHE2815D	15	±15V, 0 - 500mA

-55°C to +85°C and -55°C to +125°C
Input voltage range is 17 - 40V

MIL-STD-1772 Qualified

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Santa Clara, CA 95050
(408) 988-4930

CIRCLE NO 201

Demo disk for gate-array selection

The Vista Evaluation Software demo disk shows designers how to evaluate TGC100 Series 1-μm CMOS gate arrays. A table of allowable gate arrays and package types lets designers select the best candidate for further evaluation. For each array and package selected, the catalog on a disk provides the following information: required number of I/O, power, and ground pins; percentage of utilization of the selected array; and estimated power dissipation, using a summary of key dissipation contributors. As a final step, the demonstration disk yields design-summary information in a printout that designers can take to the company's local office for an immediate gate-array quotation.

Texas Instruments Inc, Semiconductor Group (SC-950), Box 809066, Dallas, TX 75380.

Circle No 385

Linear and custom power supplies on disk

This catalog on a disk describes a complete linear product line, including standard, custom, and tailored combinations, as well as ferroresonant and unregulated power supplies. The publication presents more than 10,000 products in a few simple tables. The 5¼-in. floppy-disk catalog runs on IBM PCs and compatibles and features pop-up help screens.

Xentek Inc, 760 Shadowridge Dr, Vista, CA 92083.

Circle No 386

Assortment of enclosures

The company's catalog reintroduces its sloped cabinet, which has been added to the Instant Optima 3-day shipping program. Other enclosures in the Instant Optima catalog include EMI/RFI shielded cabinets, vertical cabinets, the MPA (modular packing system), "Instrumate" cases, instrument cases for 19-in. equipment mounting, chassis, and a complete line of accessories.

Optima Enclosure, 2166 Mountain Industrial Blvd, Tucker, GA 30084.

Circle No 387

App note explains dc/dc power converters

This 24-pg application note addresses the basics and historical background of integrated-magnetic switch-mode dc/dc converters. The document addresses fundamental design methods for combining high-frequency transformers and filter inductances on single magnetic-core structures. The note also presents a survey of applications of integrated magnetic principles in PWM converters and resonant-converter circuits. The publication provides extensive references for magnetic design techniques.

E J Bloom Associates Inc, Product Engineering Div, 4340 Redwood Hwy, Suite E356, San Rafael, CA 94903.

Circle No 388

Handbook for DSP applications

This DSP applications handbook deals with the vendor's UT69532 IQMAC (in-phase quadrature multiplier/accumulator) pipelined processor. The book offers a brief description of the pipelined architecture and special features, such as built-in self-test. Highlighted features include array processing, math accelerators, FFT processors, digital filters, and graphics functions. Specific applications dealt with in depth are general-purpose array processing and DSP algorithms such as FIR, IIR, FFT, and DFT.

United Technologies Microelectronics Center, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907.

Circle No 389

MICE®

FORETELLS YOUR DEVELOPMENT NEEDS...

MICROTEK offers a complete line of MICE (Micro-In-Circuit-Emulator) for most popular 8, 16 and 32-bit microprocessors. These series of MICE are capable of debugging high speed targets without accumulating wait state, e.g. 25 MHz for 68020, 16 MHz for 68000/80C186. Protected Mode in 80386, coprocessor emulation in 16/32 bit series and bus/execution breakpoints in all series, are few examples of MICE powerful emulation features designed to meet advanced development needs.

All MICE series could work well with IBM PC/XT/AT*, IBM PS/2*, VAX*, μVAX*, Apollo*, Sun* and NEC* 98 series. Cross assembler/compiler, symbolic debugger and high level language debugger are also available to offer optimized software tool supports to an advanced development environment.

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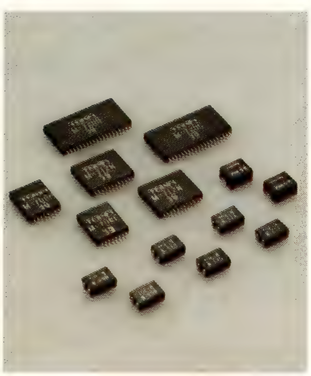

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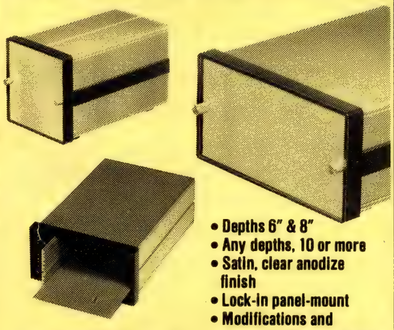

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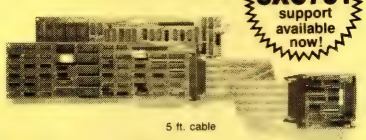

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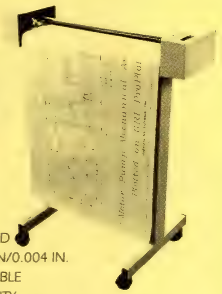

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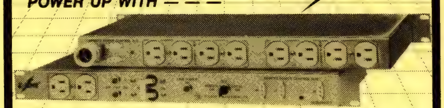

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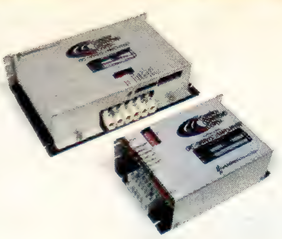

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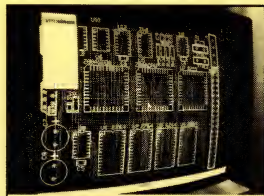

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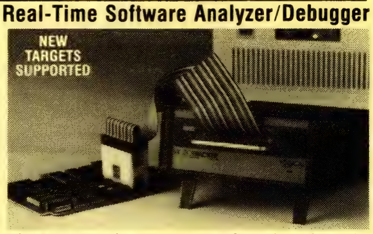

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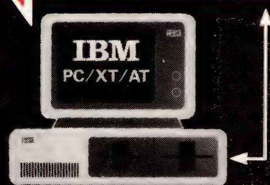

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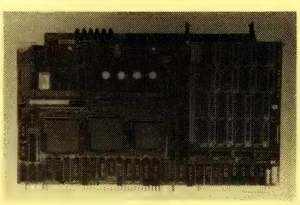

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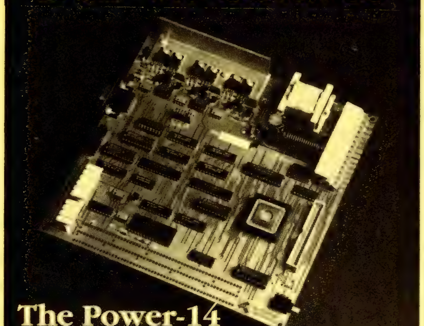

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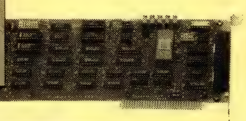

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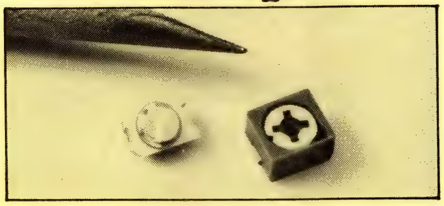

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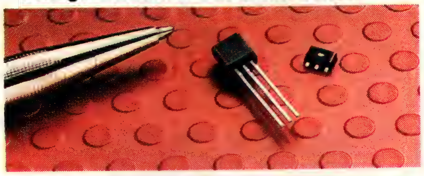

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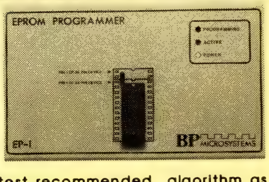

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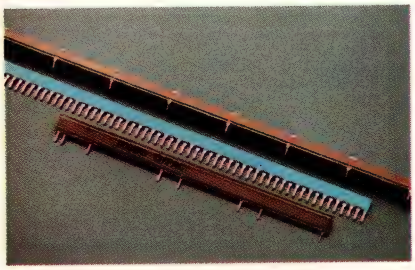

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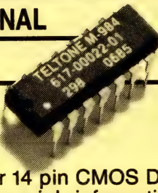

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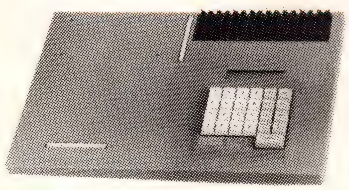

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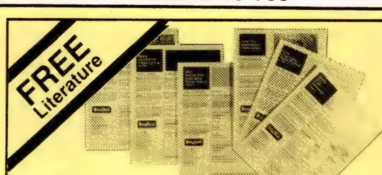

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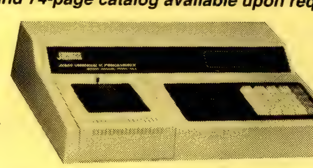

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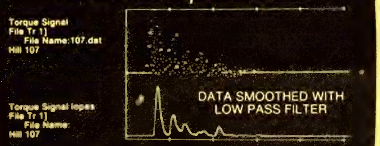

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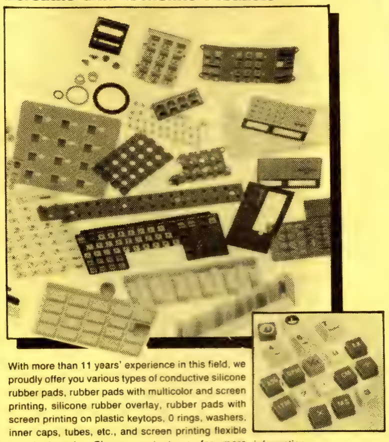

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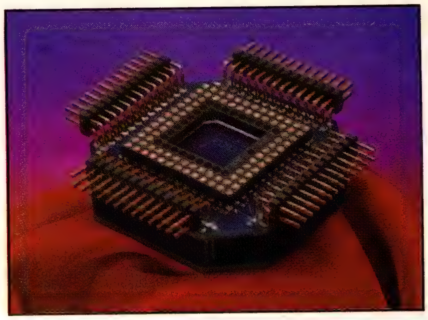

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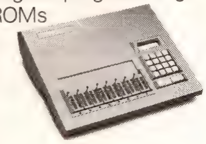

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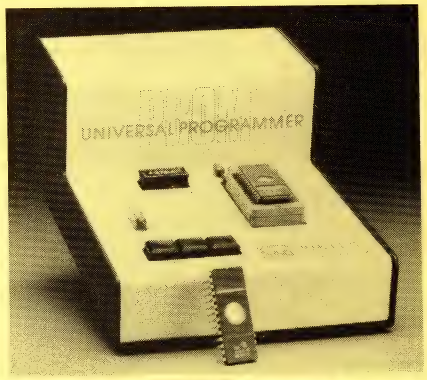

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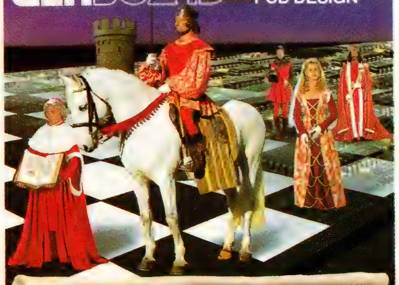

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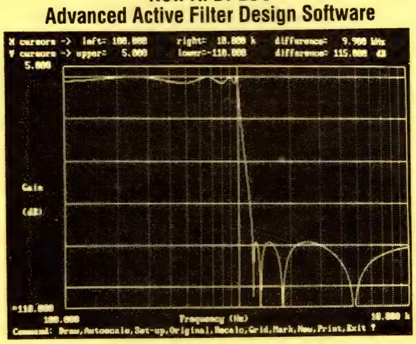

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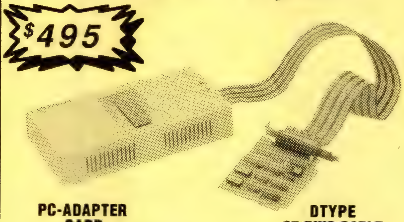

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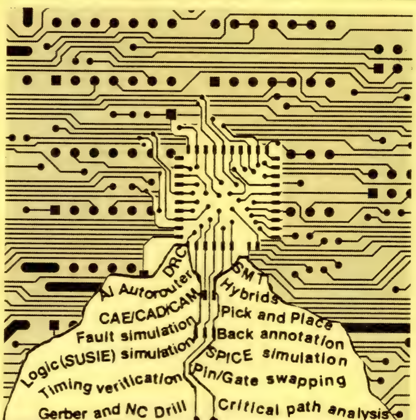

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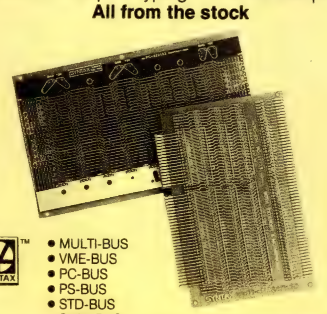

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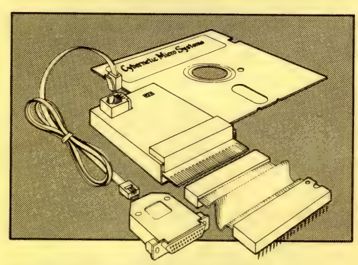

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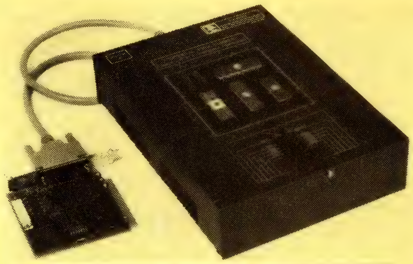

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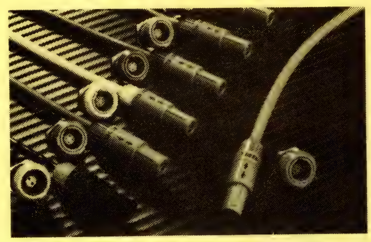

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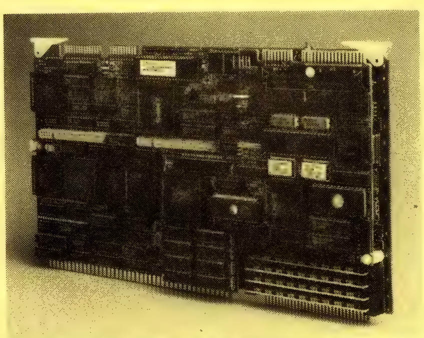

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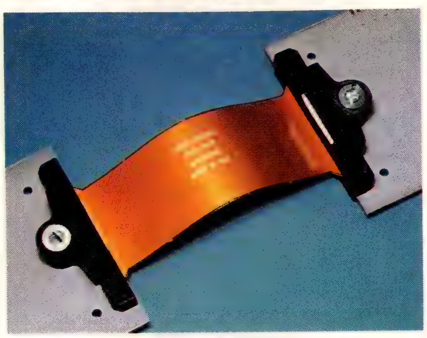

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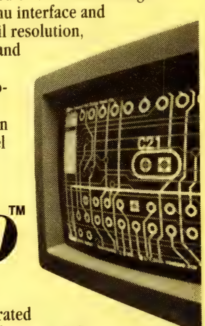

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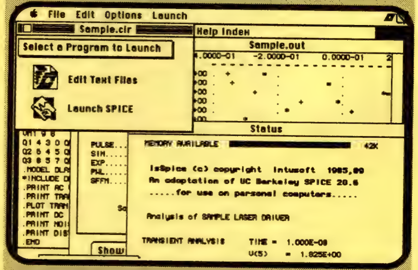

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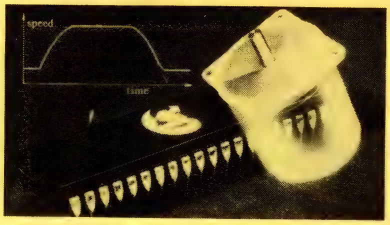

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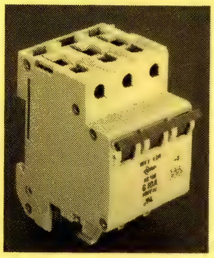

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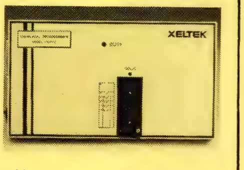

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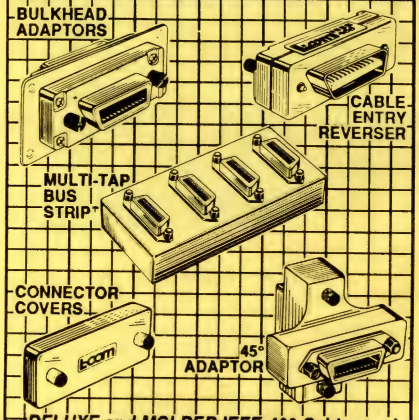

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Nov. 9	Oct. 19	CAE, Integrated Circuits	Mailing: Nov. 16
Nov. 23	Nov. 2	16th Annual $\mu P/\mu C$ Directory, Integrated Circuits	Closing: Nov. 9 Mailing: Nov. 30
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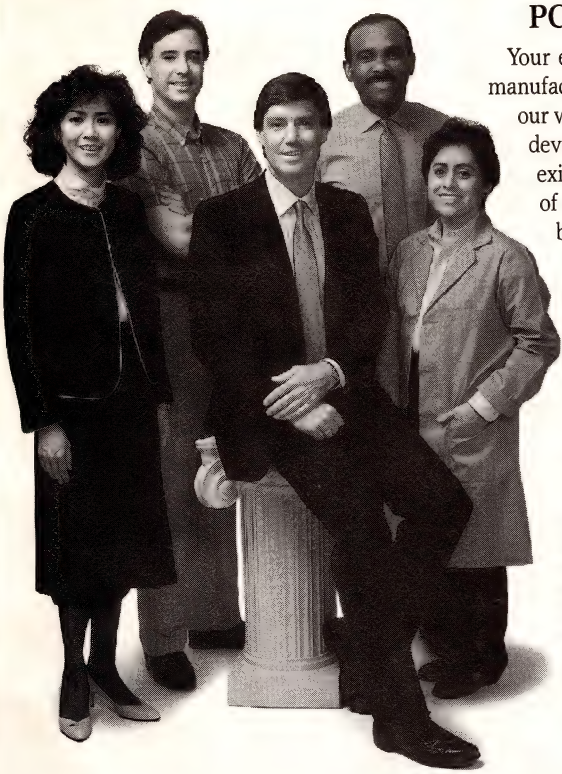

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Starting OVER

Jay Fraser, *Associate Editor*

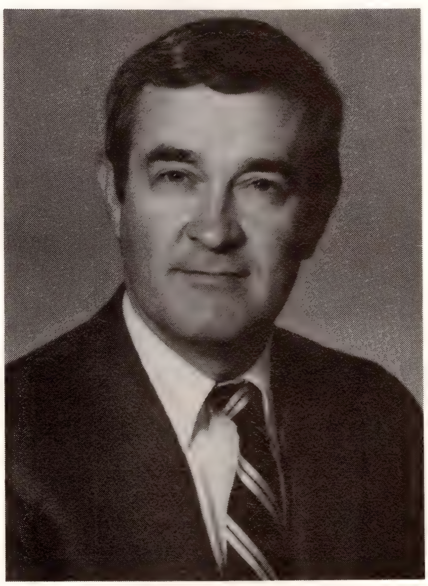
What do you do when the company you founded goes bust? You try again.

The brief history of the high-tech industry in America sparkles with success stories. We've all heard tales about people who had a brilliant idea, put together a prototype in their basement, scraped up the money to start a company, and today are millionaires.

But there are other stories not told as often. Stories about people who started their own companies, worked hard, and watched in frustration as their firms went bankrupt. What would someone whose company has expired say to someone who's considering striking out on his own?

"I would recommend to anybody who wants to start something that involves industrial automation to give me a call . . . and I'll throw some cold water on him," says Jim Smith with a laugh. He founded National Robotics in 1982, and after struggling to keep it alive for six years finally had to close it down.

Smith had a great deal of experience in business before he started his own firm. After earning his BSEE from Pennsylvania State University he joined AT&T, where he was involved in strategic facilities planning. He went on to a 12-year career at Westinghouse, eventually becoming manager of marketing development on the group level. Next he was general manager of international operations for Gould Inc, then director of strategic planning for Kulicke and Soffa Industries. At Kulicke and Soffa he wrote the business plan that persuaded the company to diversify into precision-assembly robotics. After that he helped two engineers start their own company, United States Robots. There they created one of the world's first computer-controlled assembly robots.



"Our underbelly is being eaten away by our offshore competitors, and we're going down the tubes."

JIM SMITH

At United States Robots, Smith was executive director of marketing. He helped raise more than $2 million in venture capital and planned and initiated the company's sales and marketing programs. Then he thought if I can do all this for someone else, why not for myself?

"Basically, I'd done just about everything in regular corporations, and I wanted to take a chance and see if I could do my own thing," says Smith. So in 1982, when he was 40 years old, he raised some money by taking out a mortgage on his house and founded National Robotics Inc.

"I saw the need for systems rather than robots, and that's what I started, a systems house," says Smith. National Robotics specialized in engineering and integrating robots into flexible-automation workstations.

A year after he founded it, Smith moved National Robotics to Lehigh University's (Bethlehem, PA) business incubation center. He was their first client. The business grew, but very slowly. At one time about a dozen people were associated with the company as contractors or consultants, but none of them were full-time employees.

"The first few years I was trying to do a couple of key things. I was trying to find a financial backer and I was trying to write a business plan. I ended up writing seven of them," says Smith. "I got some business, but I never got the start-up capital I needed. The bottom line is I probably tried to start too big a company with too little capital.

"If you look over the past 10 years at the automation systems companies in America, they all have a very serious common flaw," Smith continues. "In 100% of the cases they're undercapitalized, and in 90% of the cases, they don't have a good marketing effort."

Concept vs product

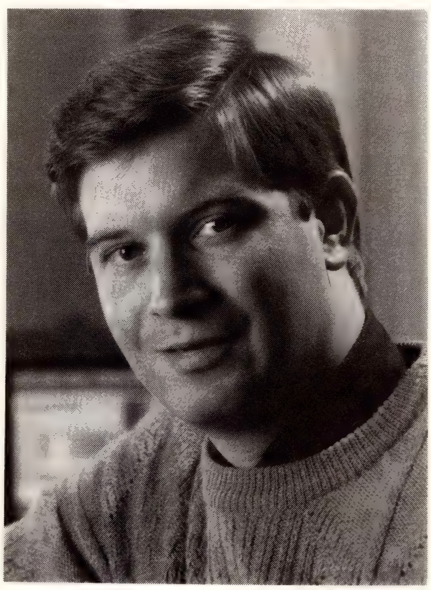
Smith says unequivocally that the most important element in starting a new company is attracting adequate financing. "Most people don't realize that people will not invest in a concept. They will only invest in a product."

Smith has written articles and given speeches about how he views the current state of business in America. "Our underbelly is being eaten away by our offshore competitors, and we're going down the tubes," he says bluntly. "I think the biggest problem with business today is the cost of money. I no longer think it's a problem of management not knowing what to do. The cost of capital is four times more for an American company than it is for our offshore competitors. Whether you're in a user side or an OEM or a supplier side, the cost of capital is killing us."

After he closed the doors of National Robotics early in 1988, Smith tried to start a cooperative productivity improvement center in Philadelphia. But before he could get it up and running, the Commonwealth of Pennsylvania initiated an $80 million not-for-profit program called Industrial Resource Centers, which did roughly the same thing as Smith's organization. "So I had to shut down my little co-op," he says. "You just can't compete with the government."

Smith warns anyone who wants to go it alone to be very cautious. "There are a lot of people who would love to start their own companies. If they want something secure, my advice is buy a franchise. Forget about developing your own brainchild, unless you can do it on the side while you're working for somebody else, so the risk is minimal."

Smith characterizes his experience of being in business for himself as "99.99% disappointment." Nevertheless, he has no intention of giving up and going back to work for someone else. He continues to develop new concepts and tries to find funding for them. He also hopes that someday he'll be able to revive National Robotics. "Believe it or not," he says, "I found one venture capitalist in America who believes in systems, and he's requested a business plan. So it's not totally dead yet."



"I got tired of fighting the same old battles and educating one set of management teams after another."

FRED DURR

Photo by John W. Keith

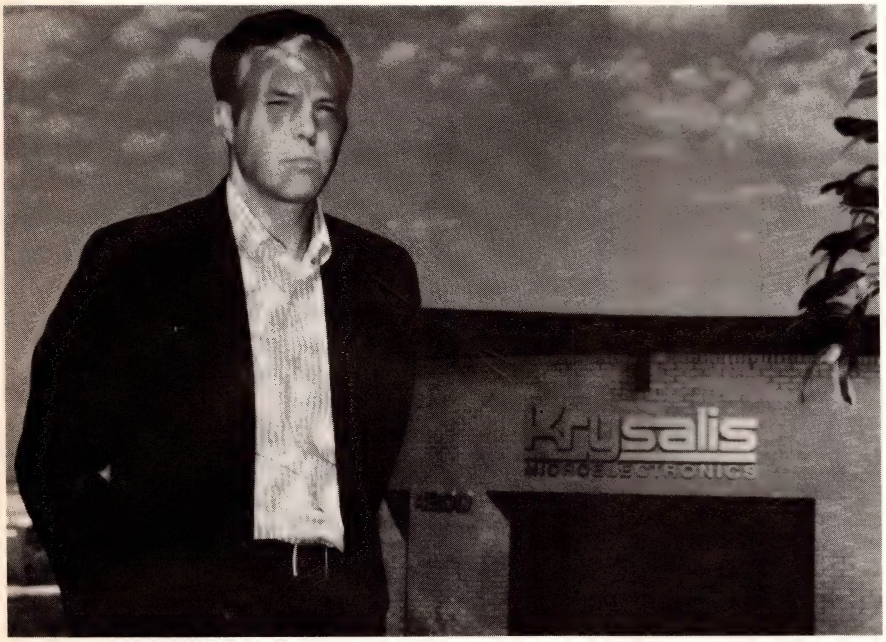
Ted Durr is a professor of sociology and history at the University of Maryland. During the 1970s he became interested in how large numbers of documents were indexed, stored, and retrieved in libraries and archives. He believed there was a better way to do it—through a text-based management system rather than the usual data-based systems. He also believed there would be a large number of customers for a better system.

Durr raised a modest amount of start-up capital from some private investors, and in 1983, along with his son Fred, who had recently graduated from Johns Hopkins University (Baltimore, MD), founded Automated Information Reference Systems Inc (AIRS). Ted Durr was the chairman of the board. His son was director of product development. They put together the first of their management teams.

The Durrs hired programmers to create the software according to their ideas and published it on floppy disks. But when they tried to market it, they found far fewer customers than they had expected. As Ted Durr says, "It was technology in search of a problem to solve."

In addition, competition was fierce. Many companies were trying

Photo courtesy of Albuquerque Journal



"Even though a big company offers some security, there can be problems there, too. You can end up being squelched."

JEFF BULLINGTON

to sell software to libraries and archives to control their documents. "The market wasn't big enough at that time," Ted Durr adds. "It still hasn't gotten big enough for all the companies that are in it. The early '90s is when I see that market maturing."

The slow start by AIRS brought pressure from the investors for a change in management. New management teams were brought in, but the situation didn't improve.

"It was constant frustration," says Fred Durr. "There were differences of opinion between management and the members of the board, who were some of the heavy investors. There were differences between management and the founders—my father and I. There were even differences among the people who were brought in at the same time as a management team."

Although AIRS did make some sales—during its best year it brought in about $250,000—it never turned a profit. The successive management teams were unable to solve its problems.

"I got tired of fighting the same old battles and educating one set of management teams after another to the market realities and the technology problems," says Fred Durr. "I had my own ideas about how to make the company successful with what kinds of expenditures at what times and at what pace the technology needed to grow. But I could never seem to get my better thoughts across."

In 1987 Fred Durr returned all his stock to the company, forgave his back wages, and formally ended his connection to the company. For a while he was still involved as a consultant, but finally left altogether.

AIRS ceased to be an independent company in February of 1989. A firm named Environmental Research Information (ERI) had been using AIRS's software and was very pleased with it. AIRS by this time was deeply in debt, and the investors wanted to sell it. ERI's subsidiary, Interactive Support Systems (ISS), bought it, and today the income it earns is used to pay off its creditors. As part of the conditions of the sale Ted Durr took a 1-year leave of absence from teaching to work full time for ISS.

Ted Durr states concisely what he thinks people should do before they try to start their own companies. "First, make sure there's a market. Second, create a business plan that will attract adequate funding. Third, hire only proven management." He believes the greatest danger for people just starting out is "the feeling that they can do it on their own."

After leaving AIRS Fred Durr started two new companies. In September of 1987 he founded Physical Dynamics Inc, which tests and measures high-temperature superconductive materials. In June of 1988, he started National Information Services Corp, which publishes full-text, bibliographic, and image database on Compact Disk-ROM.

Fred Durr says that despite the frustrations and disappointments he wasn't discouraged by his experiences at AIRS, and he never considered going to work for someone else."I guess I'm an entrepreneur through and through."

Joe Evans and Jeff Bullington met when they were officers assigned to the Air Force Weapons Laboratory in Albuquerque, NM. Evans had earned his BSEE from the United States Air Force Academy (USAF Academy, CO) and his MSEE from Stanford University (Stanford, CA). Bullington received his BSEE from Arizona State Uni-

versity and his BA in mathematics from Washington State University.

Bullington was working with electro-optic materials for high-energy laser-beam control systems. As Evans recalls, "Jeff was telling me about these magic materials that he was finding out about that had memory. And I said, 'You know, if you just took this stuff and slapped it down in a set of rows and put some columns on top of it, you'd have a nonvolatile memory, and it would probably be cheaper than dynamic RAM.' So we decided to see how far we could take this."

When his enlistment was up a short time later, Evans left the Air Force. Bullington still had two years to serve. They pooled what money they had, about $6000, and with some small loans from their parents, started their own company, Krysalis, in September of 1984.

In the beginning the company existed in Evans's garage and Bullington's apartment. Approximately a year later, they moved to the New Mexico Business Innovation Center in Albuquerque. Their research soon began to yield some very encouraging results.

"We started from scratch with the technology," says Evans, "and we were doing things at Krysalis that just hadn't been done before. We had lots of people tell us it couldn't be done, and we turned around and did it."

The first round of financing

Evans and Bullington were able to produce a film less than 2 μm thick, which had excellent ferroelectric properties, almost no defects, and was very strong. The next step was to try to join the film to silicon. But their start-up money was long gone, so they had to go out for what they call the first round of financing.

After an intensive search, the two men found five different venture capitalists willing to invest in Krysalis. They raised a total of $4.6 million. The money was absolutely essential for the continued growth of the firm, but Evans's and Bullington's equity positions dropped sharply. They were no longer in control of their own company.

Nevertheless, the future looked bright. Krysalis now employed 38 people, and it continued to make steady progress in the development of the ferroelectric memory Evans and Bullington had envisioned. By the middle of 1987, the two men felt they would be able to put a product on the market within a year. But to do that they needed a great deal of money, at least $20 million. In October they set out to find new investors. Two weeks later, on October 19, the stock market crashed.

> "Companies are a financial instrument, just like junk bonds, and they're treated as such."
>
> *JOE EVANS*

The sudden tightening of money by lenders, following the crash wasn't the only problem facing Evans and Bullington. The way venture capitalists operated had changed considerably during the 1980s.

"Venture capital wasn't really venture anymore," says Evans. "Raising money was becoming more difficult because the money being invested in semiconductor businesses just wouldn't give the kind of payoff fast enough that the venture-capital community wanted."

"Venture capitalists usually talk about a home run being a 10-to-1 return in three to five years," explains Bullington. "If you take two years to do your prototype development work, that gives you 12 months to get your manufacturing up and another two years to get your 10-to-1 return. If they've invested $20 million, then you have to get them $200 million. That's pretty strenuous for any company."

"Venture capital is not about growing companies," adds Evans. "The companies are a financial instrument, just like junk bonds, and they're treated as such."

The two men were never able to raise the money they needed. Krysalis stalled, then began to slide.

To try to reverse the downward trend, both Evans and Bullington voluntarily took substantial pay cuts. Eventually all employees had to take pay cuts. Bullington later left the staff and became a consultant in order to take his salary off the books. Nothing helped. Without the necessary large influx of capital, it was simply a matter of time before Krysalis went bankrupt.

When they founded it, Evans and Bullington owned 100% of Krysalis. By May of 1988 they owned about 6%. The board of directors showed no signs of wanting to save the firm.

"It was pretty obvious by then that we would have no control over our destinies at the company," says Evans. "No control over the return on what we had put into it up to that time. It just didn't make sense for us to stay." The two men handed in their resignations.

A few months later, the board took Krysalis into Chapter 11 proceedings. The plan that was approved by the court called for a complete reorganization and the elimination of all common stock. After complying with the court's order, the board moved the entire company to Sunnyvale, CA. By the time the move was completed, Evans and Bullington had already started a new company.

Their new firm, Radiant Technologies, is already producing two board-level products. One is a materials tester for electro-optic and solid-state applications for ferroelectric thin films. The other is the

PROFESSIONAL ISSUES

controls for a contrast-sensitivity tester.

"What we're doing differently this time is to get products out and shipped. Good products that will bring us a good revenue flow," says Bullington. "We're also doing contract research to put food on the table and give us enough money to pay for our own research. We're trying to avoid the venture-capital route."

Even after watching Krysalis slip away from them and go bankrupt, neither man has given up. "We still have a lot of technology locked up in us, a lot of creative ideas, and we want to get them out there," says Bullington. "Even though a big company offers some secutiry, there can be problems there, too. You can have all these wonderful ideas that you'd like to try to develop and you can end up being squelched. So we decided to try again."

The five people profiled here share certain obvious characteristics—creativity, a willingness to take risks, and an appetite for hard work. But they also have a common way of thinking that may not be apparent at first. When their companies failed, not one of them gave up his independence and joined a giant corporation, and not one of them threw in the towel and ran away to the South Seas. They never considered those as serious alternatives, if they thought about them at all. After their companies went under, they buckled down and started new companies. Perhaps that's one of the keys to success. If you want to start your own company, you should also be prepared to start again. EDN

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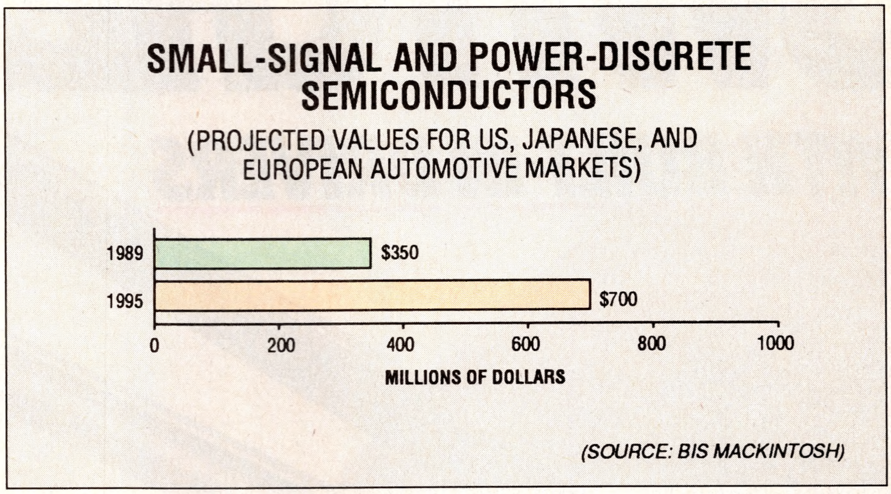
EDITED BY JAMES P SCANLAN

Automotive market grows for discrete semiconductors

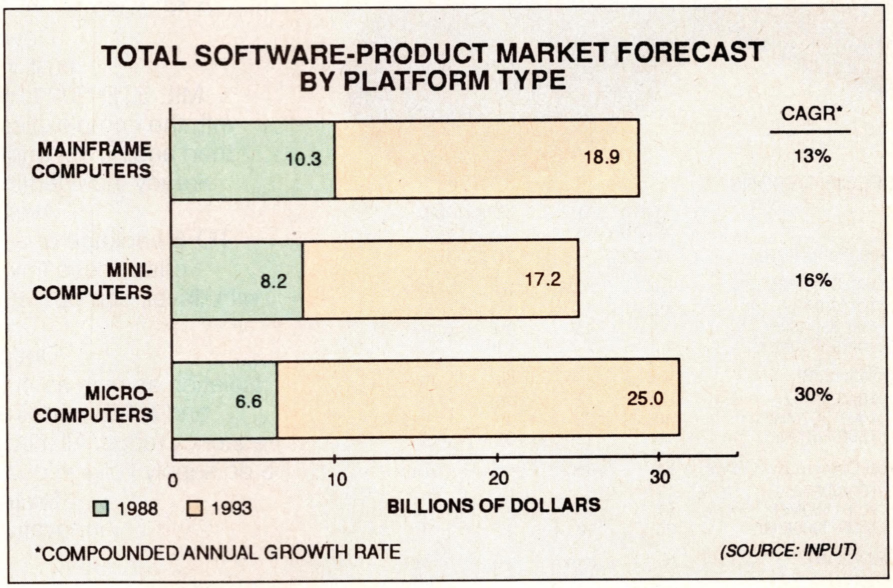


Suppliers of discrete semiconductors to the automotive industry can look forward to sustained market growth over the next five years, despite the electronics trend toward greater integration, according to a report published by BIS Mackintosh (Luton, UK). The automotive market value for small-signal and power-discrete semiconductors in the US, Europe, and Japan, is expected to reach $350 million this year. An average annual increase of 12% of this figure is predicted into the 1990s. By 1995, the figure is expected to exceed $700 million.

The wide use of electronic systems in automobiles will overshadow any market erosion caused by the emergence of integrated solutions such as smart-power devices, custom chips, and multiplexed wiring systems, the report states. The biggest growth area for discrete semiconductors is in power-switching transistors, where annual growth could reach 25% by 1995.

In Europe, stricter emissions-control laws will increase demand for power transistors in fuel-injector solenoid drives and electronic-ignition control modules. In the US, power-transistor growth will be aided by the increased appearance of convenience features, such as power seat adjust, suspension control, and power window lifts.

Software market will grow to $36 billion by 1993



User expenditures for software products (both applications and systems software) will increase to $61.1 billion by 1993, according to a report published by Input, a Mountain View, CA-based market-research firm. Expenditures for last year were $25.1 billion.

Expenditures for mainframe-system software will grow by $18.9 billion. Figures for minicomputer-system and microcomputer-system software are $17.2 billion and $25.0 billion, respectively.

The report estimates that the software-products market will have the largest growth rate of any information-service segment; that is, 20% over the next five years. Input defines the information-services industry as six delivery modes: software products, processing services, network services, turnkey/value-added-reseller systems, professional services, and systems integration.

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Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
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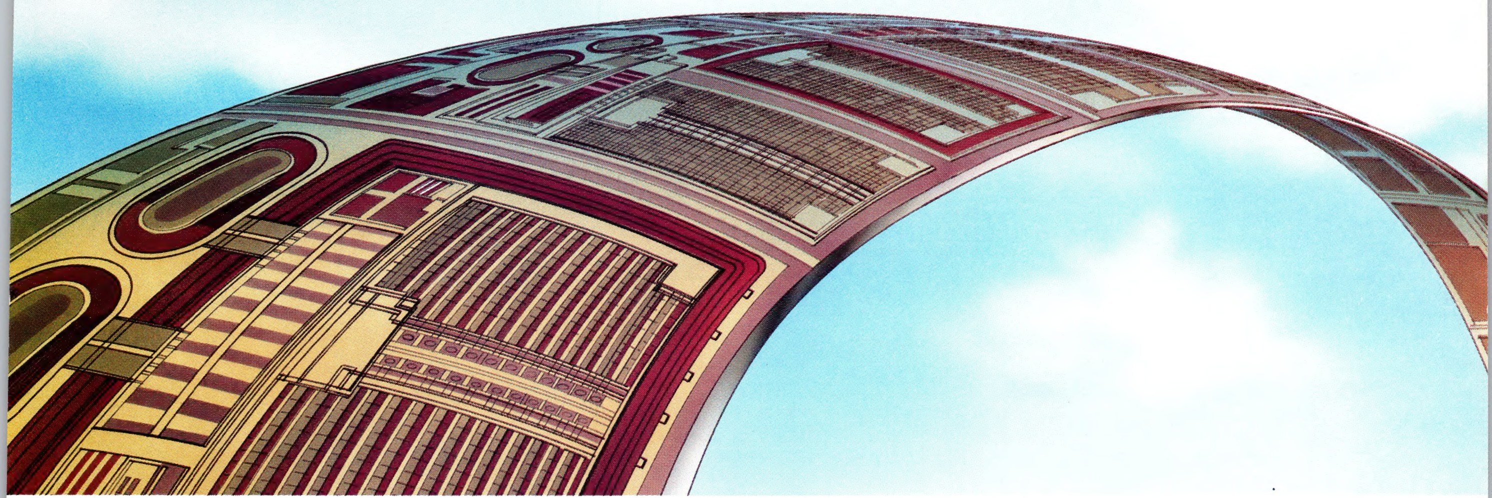

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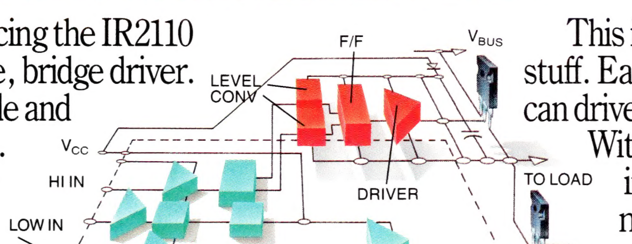

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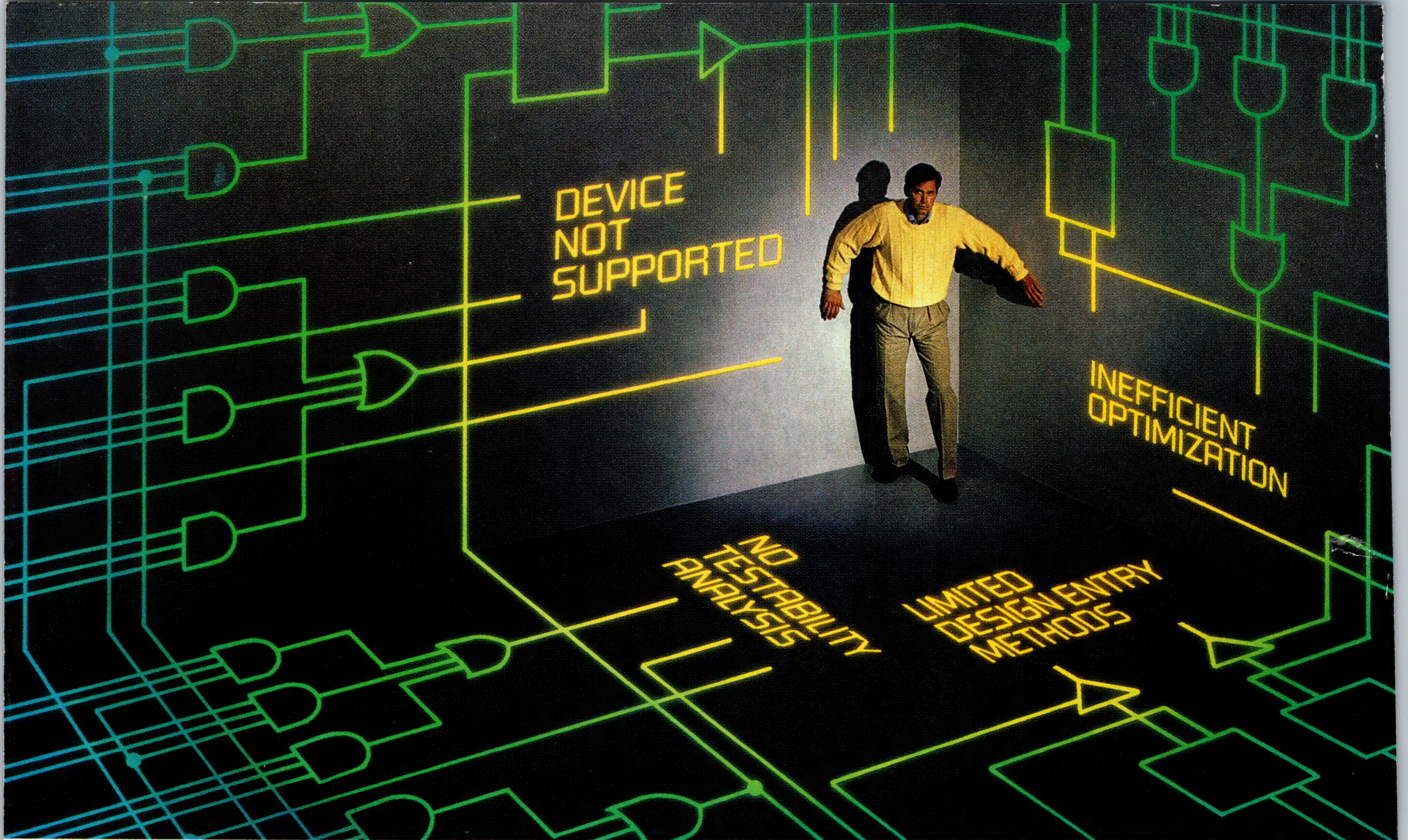

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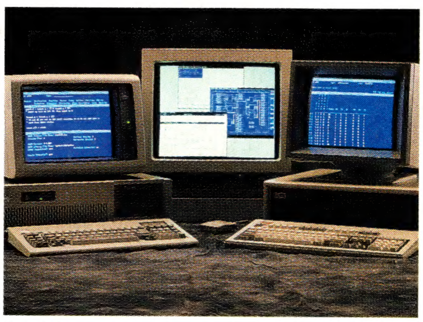

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